

2023

Salishan Conference on High Speed Computing

sgcardw@sandia.gov

Neuromorphic **Computing:** How the Brain can inspire computing from HP to the Edge

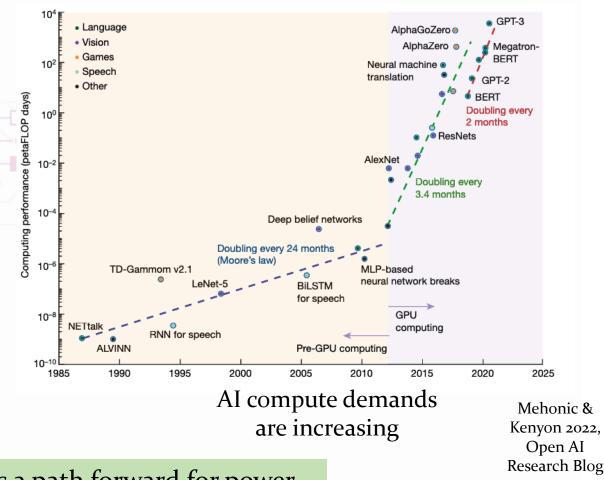
> Suma George Cardwell Cognitive and Emerging Computing Sandia National Laboratories

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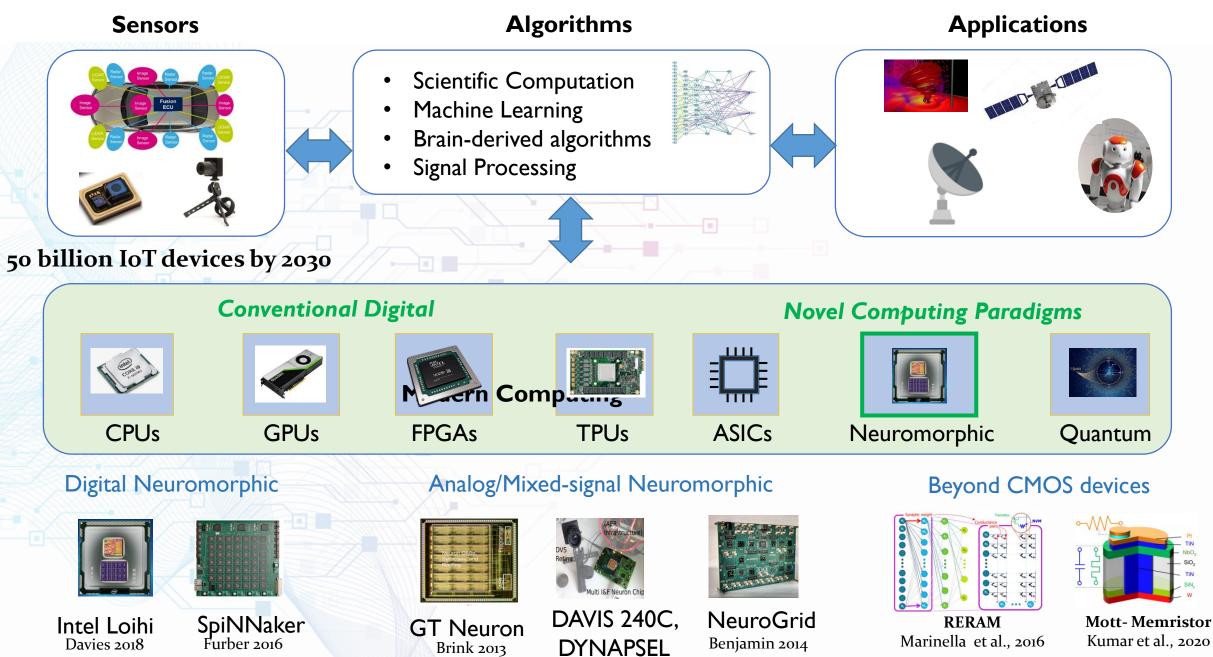
FUNDAMENTAL CHALLENGES IN COMPUTING

- Limits of scaling have ushered in the "Golden Age of Computer Architecture" Hennessy & Patterson 2019
- Inefficiency of generality
- Performance saturation



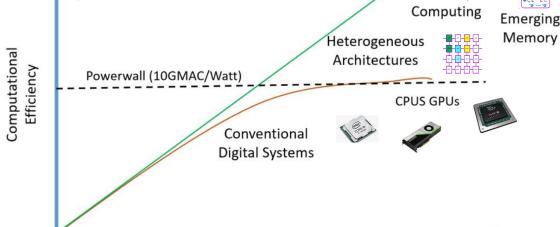
Neuromorphic Computing gives a path forward for power efficiency scaling and meeting future computing needs.

COMPUTING LANDSCAPE

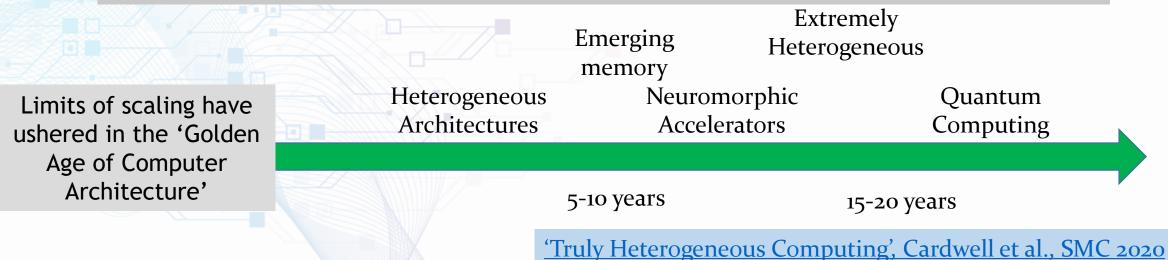


FUTURE OF COMPUTING: HETEROGENEOUS

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Co-Design is critical to build the next-generation heterogeneous systems



NEUROMORPHIC COMPUTING: INSPIRED BY THE BRAIN

Brain and Computing: Why make the connection?

- High computational efficiency, Single neuron ~1MMAC/pW
- Processing and memory operations performed by the same components
- Self-organizing system
- Online learning
- Solving ill-structured problems
- Transfer learning
- Spiking/event driven communication, subthreshold computation

Neuromorphic techniques will be disruptive to how we develop our computing systems

Neuromorphic techniques

1MMAC/(s)/mW

1MMAC/(s)/uW

Analog/ Compute-inmemory techniques

Hasler 2016



NEUROMORPHIC COMPUTING

Stanford Neurogrid

Digital Neuromorphic

Analog/Mixed-Signal

SNL hosts Intel's 5 million neural supercomputer Scaled to a billion neurons Scaled to a billion neurons Image: Scaled to a billion neurons

RRAM Crossbar

neurons

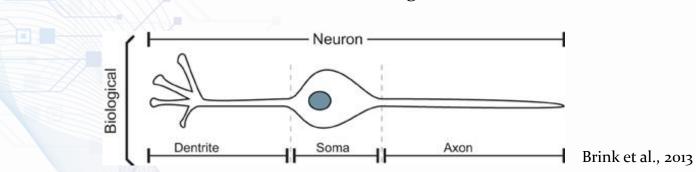
SpiNNaker/ SpiNNaker 2

Intel Loihi/

Loihi 2.0

IBM TrueNorth

ODIN (Open-source)



NeuRRAM

UCSD/Tsinghua

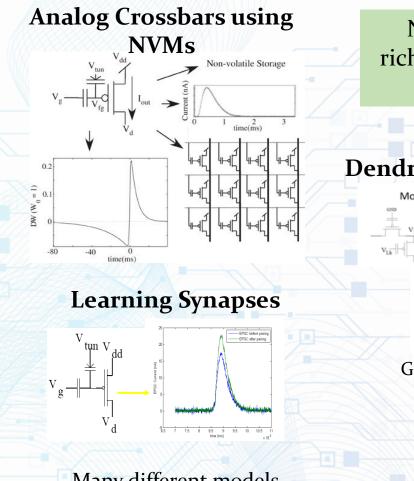
SHE write curren

MTJ

Assist field

Beyond CMOS Devices

NEUROMORPHIC BUILDING BLOCKS

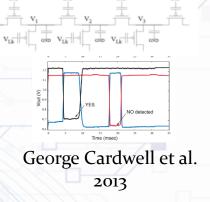


Many different models for neurons, synapses, online learning and dendrites.

Neuromorphic offers computational richness we can leverage, to move beyond today's computational limitations.

Dendritic Processing

Modeling using CMOS transistors



Cochlea

Analog BPF:

:

Silicon Cochlea

Liu et al. 2020

Event Encoders

AAAA → |||||||

Event-Driven

Processo

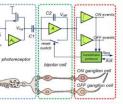
Planning

Neural Path

Koziol et al. 2013

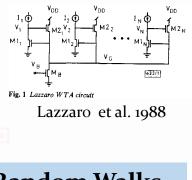


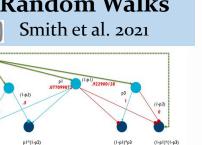
Silicon Retina/ Event Sensor



Posch et al. 2014







Delbruck et al.

2020

2 in



Scientific

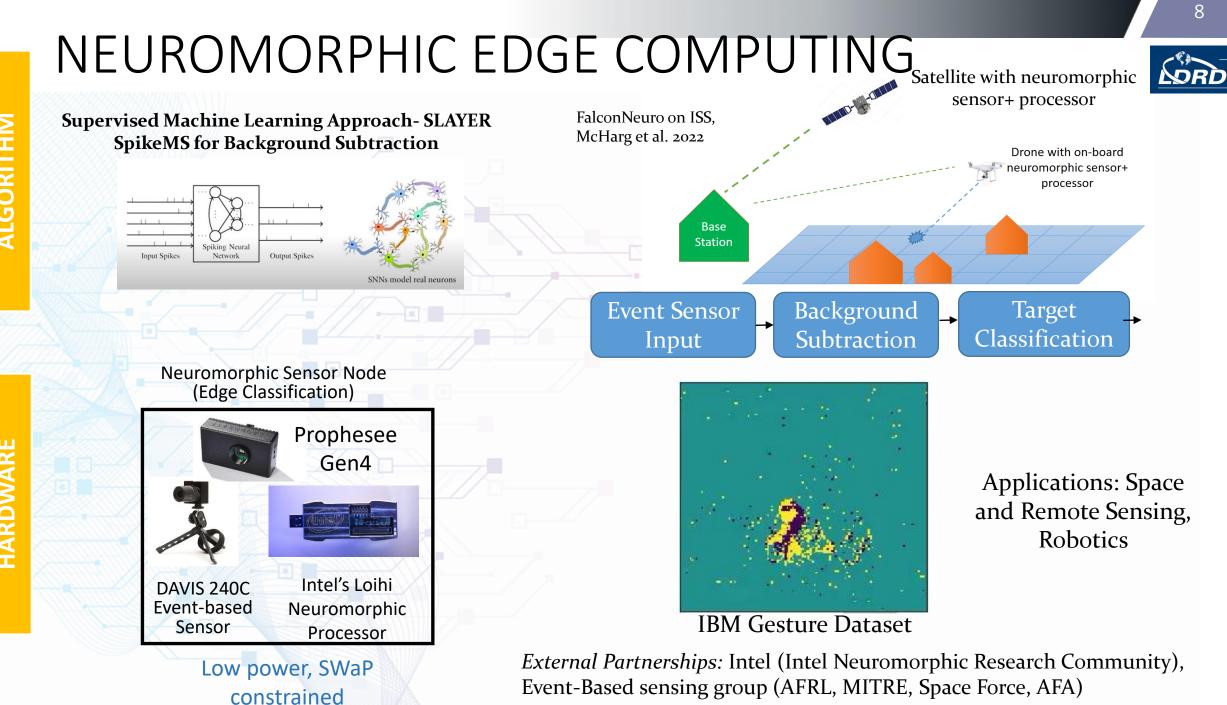
Computing

APPLICATIONS

AI/ML (ANN, SNN)

Brain-inspired

algorithms



ALGORITHM

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HARDWARE

8

SpikeMS: Prophesee Driving Data



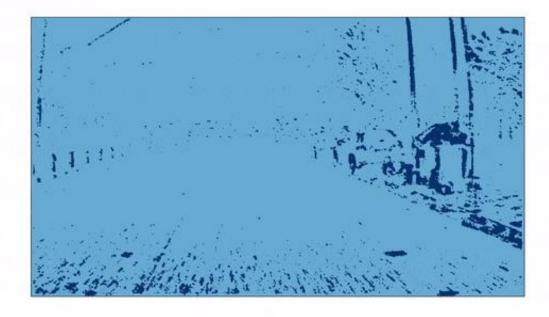
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Prediction



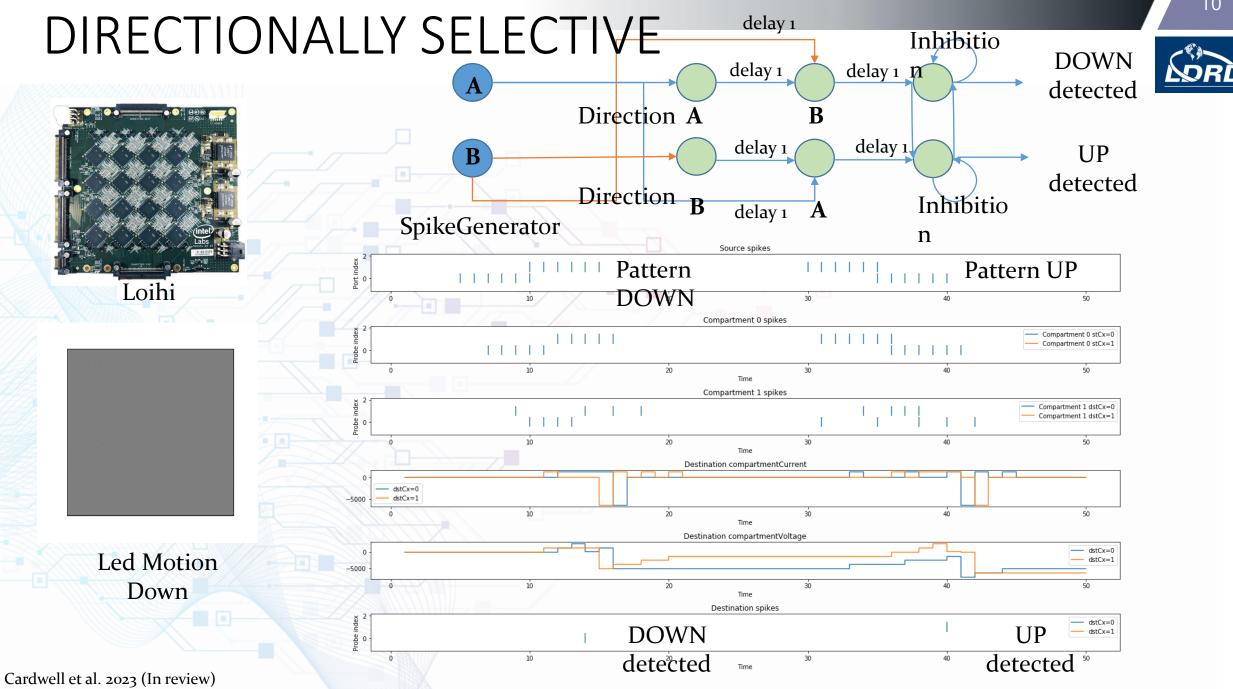
Input

Prophesee Event Sensor Output

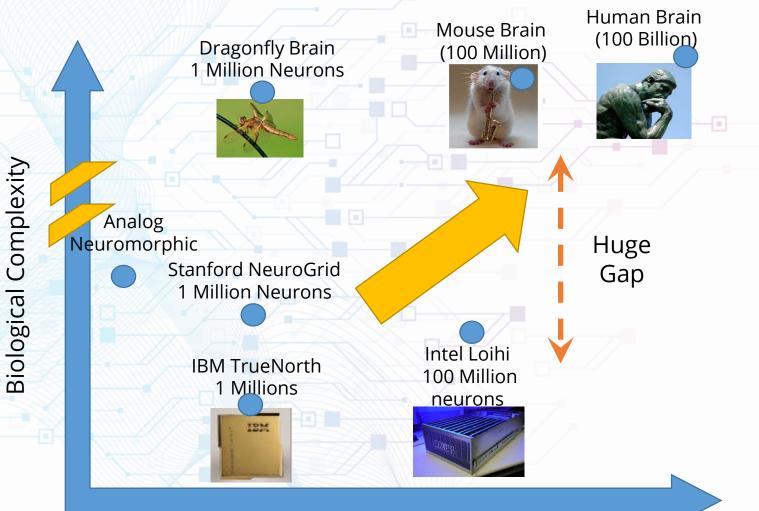


Post-SpikeMS removing most background information

SpikeMS: Parameshwara et al. , IROS 2021



NEUROMORPHIC COMPUTING CHALLENGE: SCALABILITY VS. COMPLEXITY



- However, to achieve brain-like complexity we need both scaling and rich dynamics.
 - Solving ill-structured problems
 - Online learning
 - Transfer learning

Understanding fundamental mechanisms in neuroscience, translated to algorithms and models will influence nextgeneration devices, architectures and intelligent computing systems

Scalability (# of Neurons, Synapses)

INCREASING "BIOLOGICAL COMPLEXITY"

Increase computational efficiency and Increase computational density

Novel devices and materials can help bridge this gap.

LIF neuron

- Single passive compartment
- Spikes
- Limited dynamics
- Relatively easy to scale

LIF: leaky Integrate and Fire

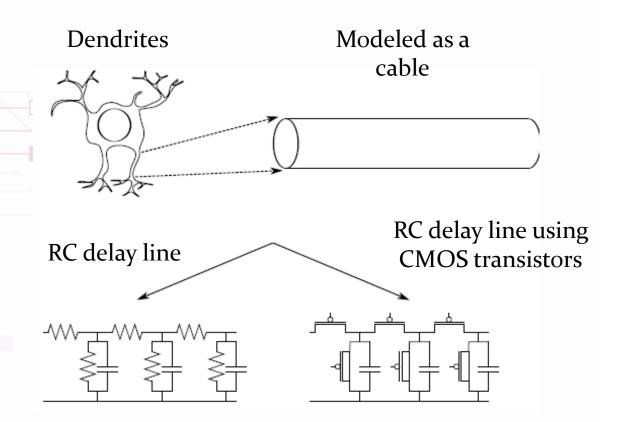
Biological neuron

- Dendrites = intricate structure and dense connectivity
- Complex pattern of active conductances
- Rich dynamics , multiple patterns of spiking, subthreshold computation
- More computational power, not compact

MODELING DENDRITES

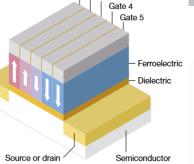
- Dendrites are tree-like structures that connect neurons synapses to its soma.
- Dendrites are not wires!
- They can perform interesting computation like
 - Coincidence Detection
 - Current Summation
 - Directional selectivity
 - Non-linear filtering
 - Amplification of Synaptic inputs

London 2005, Hausser 2003



Nease et al. 2011

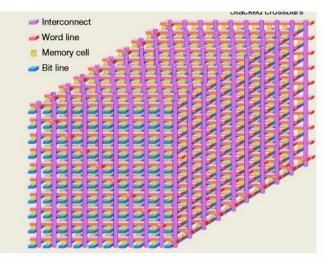
WHY IS THIS USEFUL?



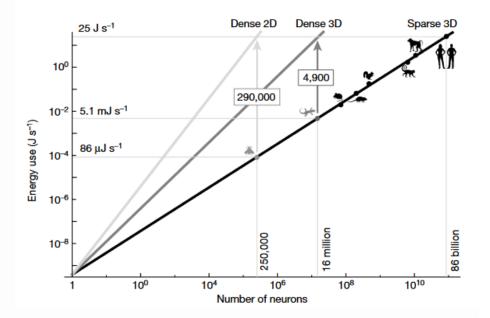
Gate 2 Gate 3

- Dendrites perform non-linear computation like a multi-layer NN enabling "neuron within a neuron"
 NanoDendrite Multi-gate FeFET capability.
- Footprint of dendritic circuits smaller compared to a neuron circuit.
 - Dendrite (1-2 transistors with sub-threshold FGs) [George 2013], HH Neuron circuit (7-8 transistors)[Farquhar and Hasler], LIF (8-10 transistors) [Indiveri 2011]
 - Proposed multi-gate FeFET for dendrites with 3D stacking for dense connectivity [Kwabena, Nature 2022], Energy estimated to program device ~29.6fJ/event [Saha et al., 2021]

• Computing in the interconnect, more energy efficient computation



Dendrocentric Learning- Kwabena, Nature 2022





DRAGONFLY EXAMPLE



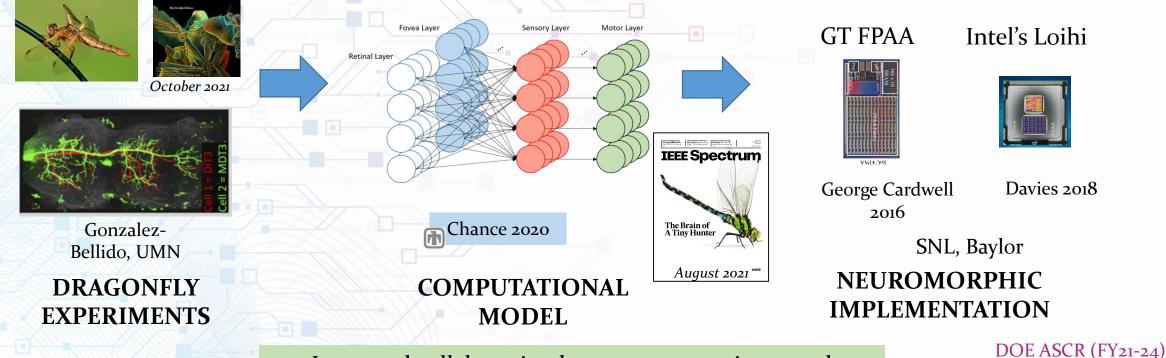
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Algorithms Devices &

Physics of Computing

Coordinate transformations from Dragonflies to Neuromorphic Hardware

Lead PI: Frances Chance, SNL

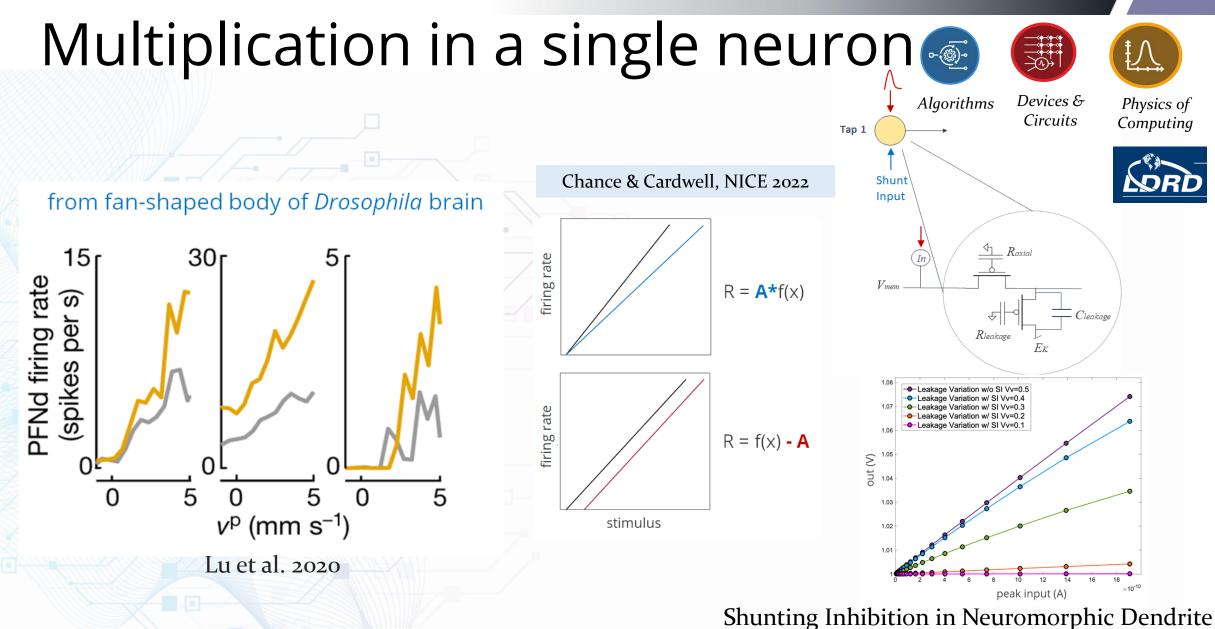


Increased collaboration between neuroscience and neuromorphic engineering will facilitate development of novel neural-inspired architectures.



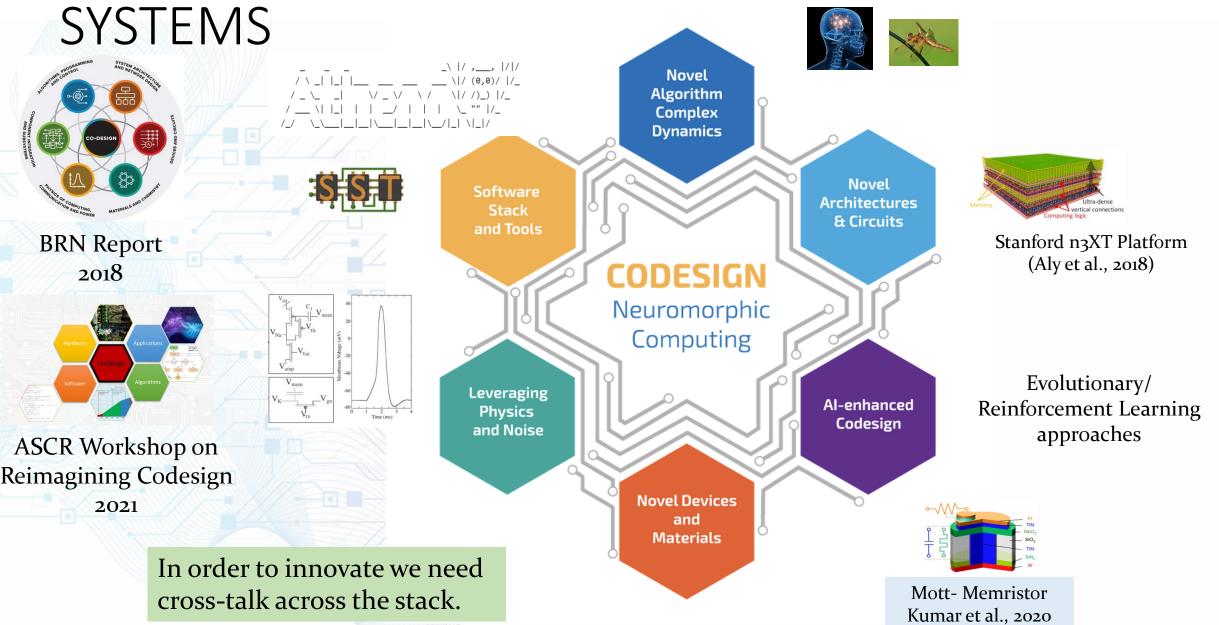
Department of Energy

Advanced Scientific Computing Research



Collaborators: University of Texas at Austin, Intel Neuromorphic Research Community

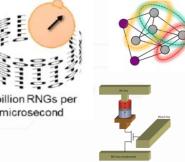
NEXT-GENERATION NEUROMORPHIC



CODESIGN IS CHALLENGING

Co-Design Tools for Novel Architectures

PODOU Next-generation Neuromorphic Architectures





ATHENA Analytical Tools for analog and neuromorphic ML accelerators

ASC-AML (FY20-22) Advanced Simulation & Computing -Advanced Machine Learning

Al-enhanced Codesign Reinforcement Learning/Evolutionar y methods for Circuit and System design

AS&T LDRDs (FY21-23) Advanced Science & Technology Laboratory Directed Research and Development

COINFLIPS

Probabilistic Neural Computing, Leverage stochasticity in beyond-CMOS devices

> DOE ASCR/BES (FY21-24) Department of Energy

Advanced Scientific Computing Research Basic Energy Sciences

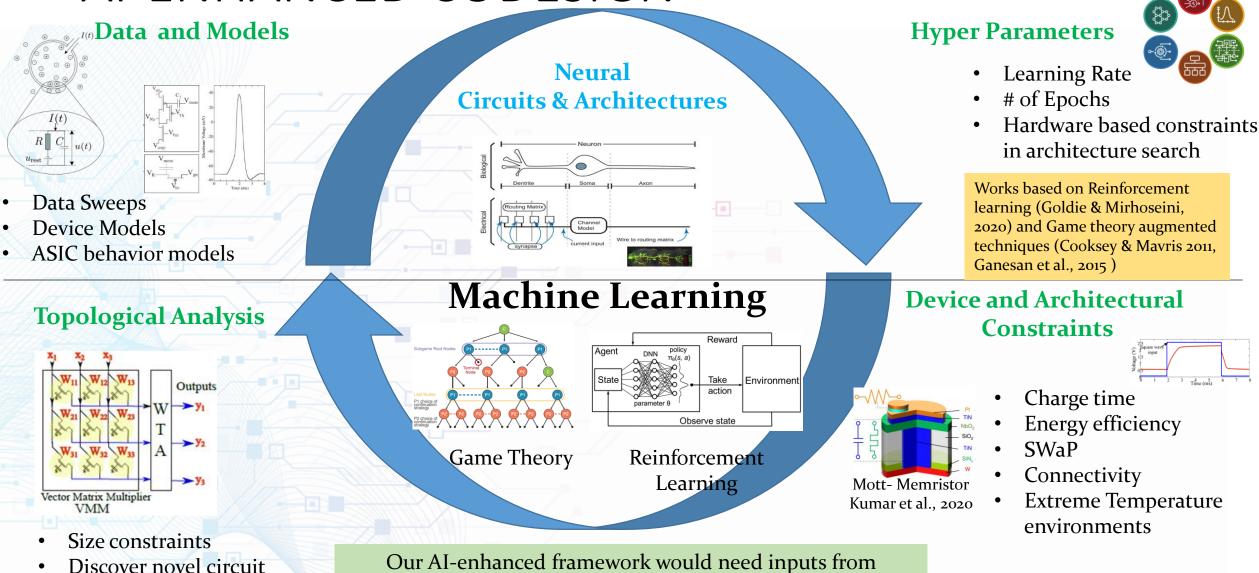
DRAGONFLY

Dendritic processing, Coordinate transformation from Dragonflies to Neuromorphic hardware, Analog and digital

> DOE ASCR (FY21-24) Department of Energy Advanced Scientific Computing Research

External Collaborators: UT Austin, Intel, Infineon Memory Solutions, Georgia Tech, UMN, Baylor University, UT Knoxville, Temple University, NYU, ORNL

AI-ENHANCED CODESIGN



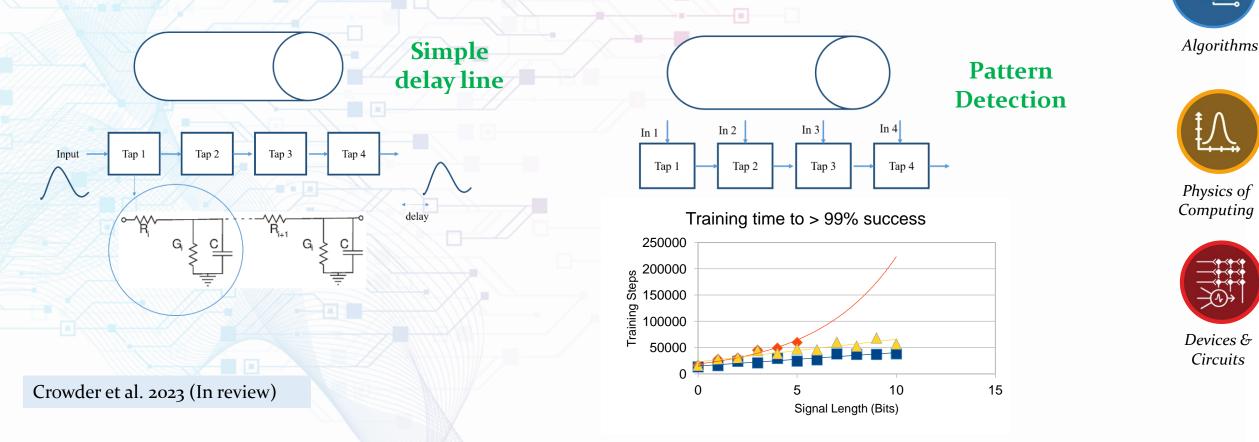
topologies

Our AI-enhanced framework would need inputs from algorithms, devices, architectures and ML-based hyperparameters. The framework will enable new capabilities.



AI-ENHANCED CODESIGN: NEURAL CIRCUITS

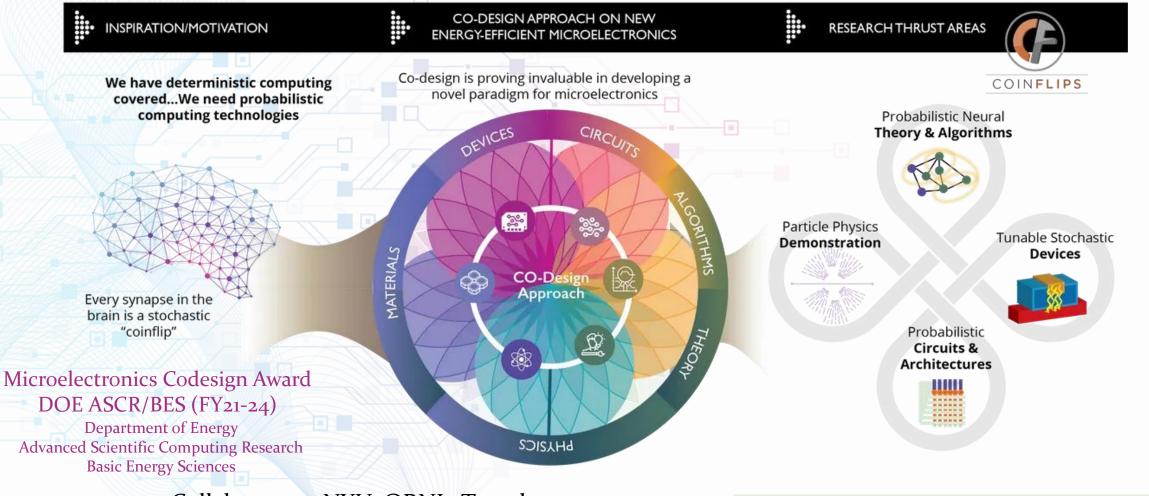
We developed an RL algorithm approach which is capable of building very simple circuits.





AI-ENHANCED CODESIGN: COINFLIPS

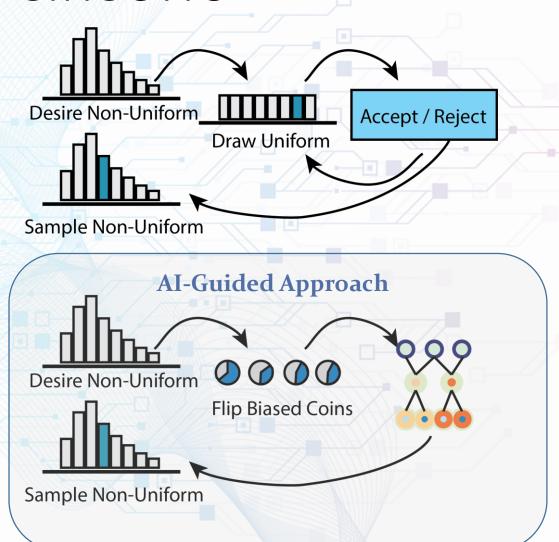
Lead PI: Brad Aimone



Collaborators: NYU, ORNL, Temple University, UT-Austin and UT-Knoxville

https://coinflipscomputing.org/

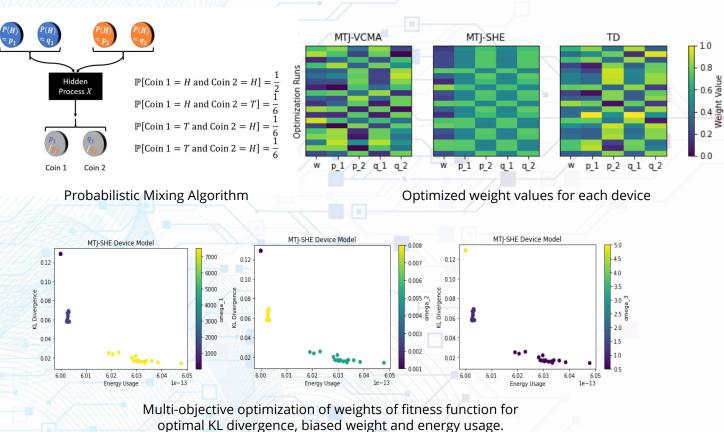
AI-GUIDED CODESIGN OF PROBABILSITIC CIRCUITS • Unfair coins can be combined with



- Unfair coins can be combined with AI-designed neural circuits to allow sampling of application desired probability distributions, avoiding accept/reject steps.
- We leveraged evolutionary algorithms for circuit design and optimization
 - **LEAP** (Library of Evolutionary Algorithms in Python)
 - **EONS** (Evolutionary Optimization for Neuromorphic Systems)- Schuman et al. , 2020
- We used abstracted device models for TD and MTJ to capture functionality and energy usage.

Cardwell et al., International Conference on Rebooting Computing (ICRC) 2022

AI-GUIDED CODESIGN OF PROBABILSITIC CIRCUITS



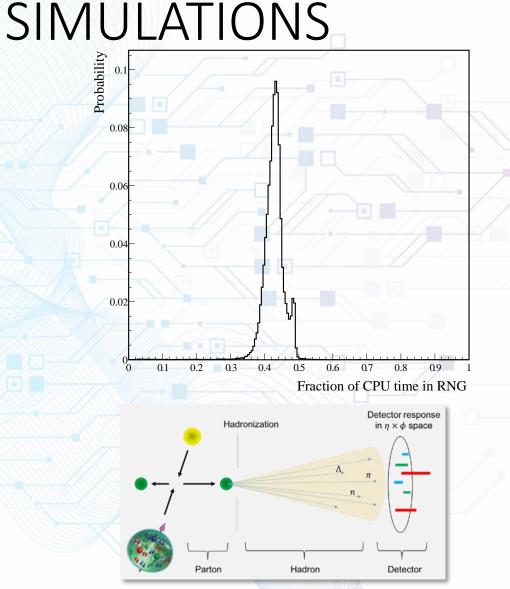
Cardwell et al., International Conference on Rebooting Computing (ICRC) 2022

- Weights are customized for the device's behavior to target the best performance in terms of KL divergence and energy usage.
- One of the challenges in optimizing for both algorithms and devices was appropriately abstracting the device models and algorithmic constraints.
- The functional models developed will also be evolved in time as new device data and research emerges.
- Our framework can accommodate any emerging device type.

COINFLIPS APPLICATION: NUCLEAR PHYSICS



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- For a particular collider physics simulation [Pierog et al., Phy Rev. 2022], ~ 270K pseudo- random numbers needed for a single event, with billions of events needing to be simulated.
- CPU time is ~ 30-50% of the total compute time
- Direct random number generation leveraging stochastic devices can promise significant energy savings for such applications

Misra et al., Advanced Materials 2022

Random numbers are a limiting computational cost for some nuclear physics applications

COINFLIPS APPLICATION: NEUROMORPHIC



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- MAXCUT HT ... 100101 HT ... 101001 HT010110 HT ...011101 Loihi vs. Solver solver 8000 Ioihi - random weights 6000 Conut 4000 2000 0 2000 2200 1600 1800 2400 Cut Weight
 - Loihi generated graph cuts of neuromorphic GW algorithm match conventional MAXCUT solver generated cuts.
 - Results demonstrate effective implementation on current neuromorphic platform with minimal loss and potential to take advantage of future accelerated neuromorphic platforms.
 - MAXCUT has broad real-world applications ranging from circuit design to power grid resilience, and these applications are well positioned to take advantage of dramatically accelerated neuromorphic implementations.

Theilman & Aimone, *Neuro-Inspired Computational Elements Conference* (NICE 2023)

Loihi generated graph cuts of neuromorphic GW algorithm

26 AI-ENHANCED CODESIGN ACROSS SCALES Algorithm Design Device Design **Circuit Design** System Design Architecture Design In-Memory Computing Cluster Controller In-Memory Computing Unit Memory & Logic Memory & Logic Fan (UCF), 2018

Can we leverage AI to generate specifications for novel devices?

Approach

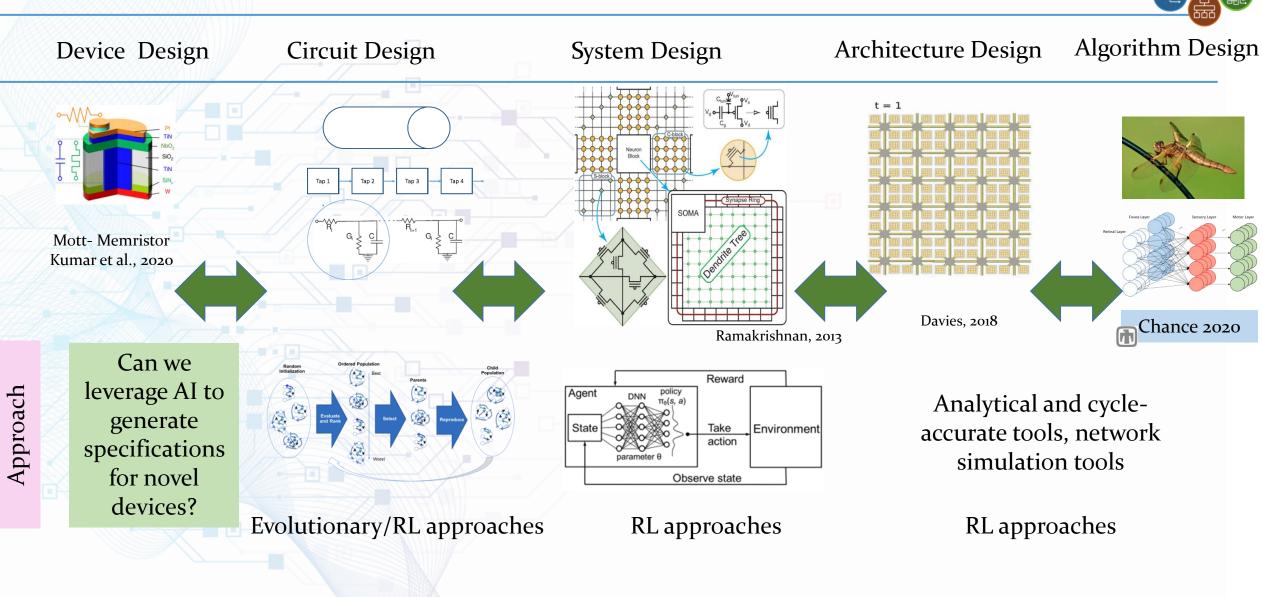
Agent DNN State Evolutionary/RL approaches RL approaches

Reward policy Take Environment action Observe state

Analytical and cycleaccurate tools, network simulation tools

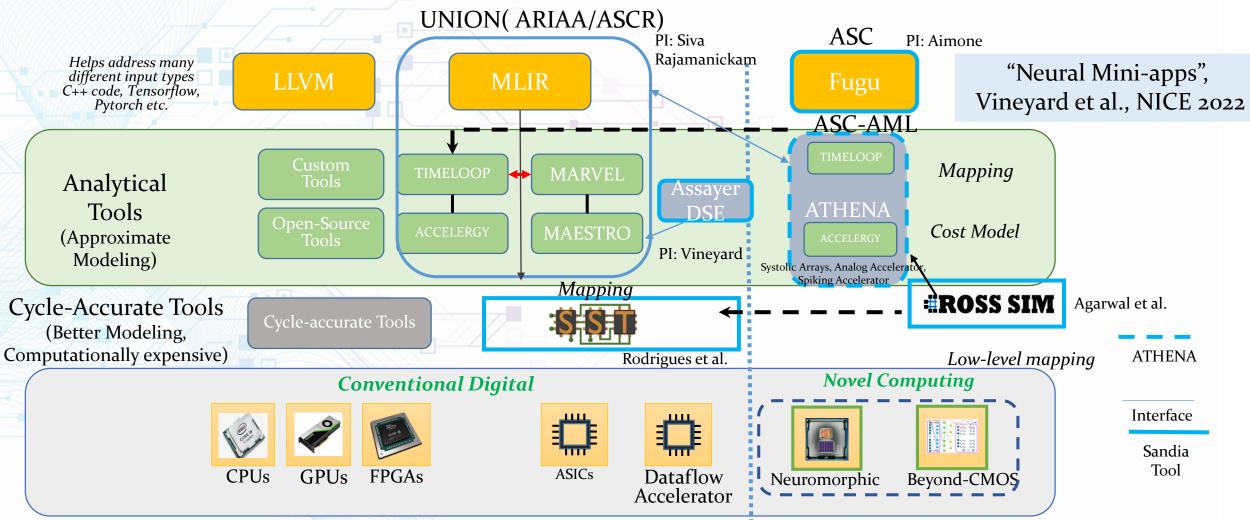
RL approaches

AI-ENHANCED CODESIGN ACROSS SCALES



CHALLENGE: SOFTWARE TOOLS

• ATHENA (Analytical Tool to evaluate Neuromorphic Architectures) will be leveraged to do design space exploration of novel architectures that leverage neuromorphic and emerging devices.



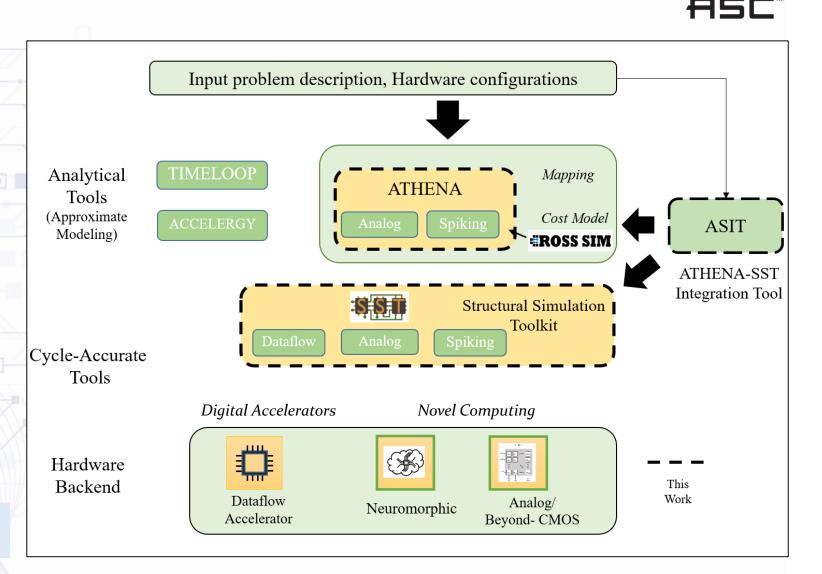
ATHENA

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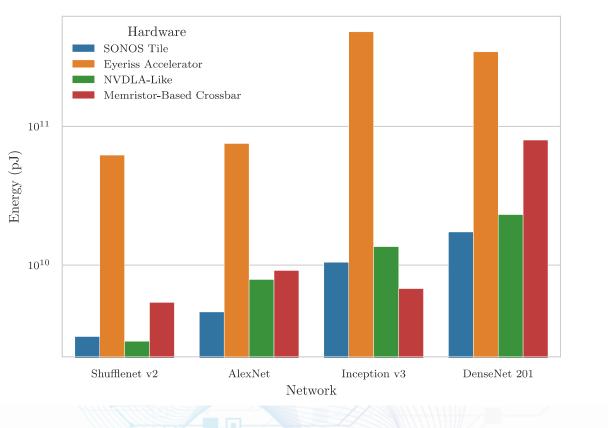
(Analytical Tool to Evaluate Heterogeneous Neuromorphic Architectures)

- ATHENA will quickly evaluate performance metrics of analog architectures
- Developed as part of a larger ecosystem
 - Tools to enable nextgeneration hardware design prototyping

Plagge et al., International Conference on Rebooting Computing (ICRC) 2022



ATHENA – HARDWARE PERFORMANCE



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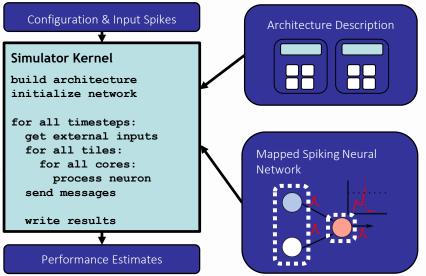
Plagge et al., International Conference on Rebooting Computing (ICRC) 2022

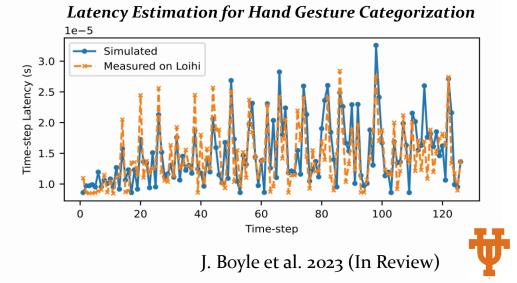
- ATHENA was used to compare the performance of multiple hardware devices against various deep learning networks
- The SONOS tile-based architecture performed well across networks, with one notable exception: the Inception v3 network
- This performance difference could be explored – showing ATHENA's potential for codesign work

SANA-FE: NEUROMORPHIC SYSTEM MODELING & CODESIGN

- Tools are needed to rapidly estimate performance of neuromorphic architectures for design-space exploration
- General & extensible spiking H/W simulator
- Model functional behavior & track
 performance
- Schedule messages & intra-core interactions
- Calibrate simulator to real-world systems
- Accurately predicts latency & energy of gesture categorization spiking neural network (SNN)
- Faster than existing simulator (NeMo)

SANA-FE: Simulating Advanced Neuromorphic Architectures for Fast Exploration





SANA-FE: NEUROMORPHIC SYSTEM MODELING & CODESIGN

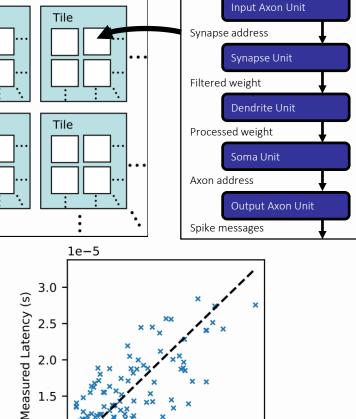
SANA-FE: Simulating Advanced Neuromorphic Architectures for Fast Exploration

Tile

- Neuromorphic system architectures
 System design space exploration
 Spiking Neural Network-based H/W
 - Novel features e.g., analog compute
 - Modeling & benchmarking for codesign
- Fast spiking H/W simulation
 - General & extensible framework
 - Functional model & performance
 - Calibrate simulator to real-world H/W
 - Accurately estimate latency & energy

•





2.0

2.5

Simulated Latency (s)1e-5

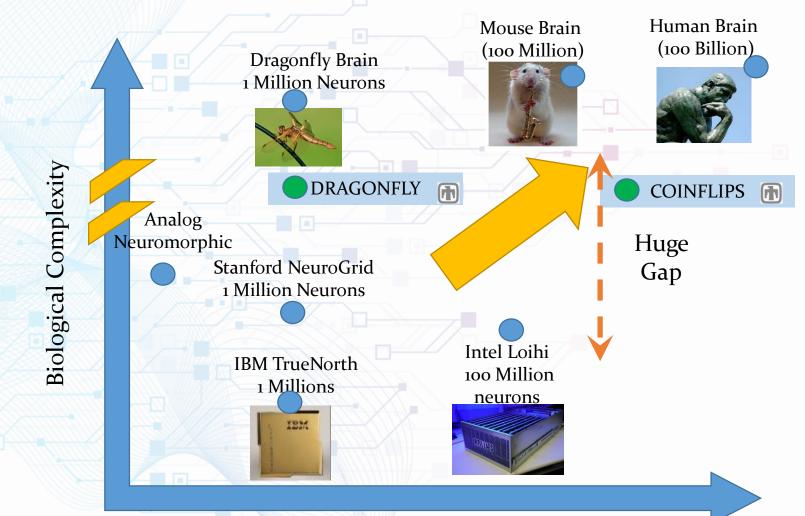
J. Boyle et al. 2023 (In Review)

3.0

Core



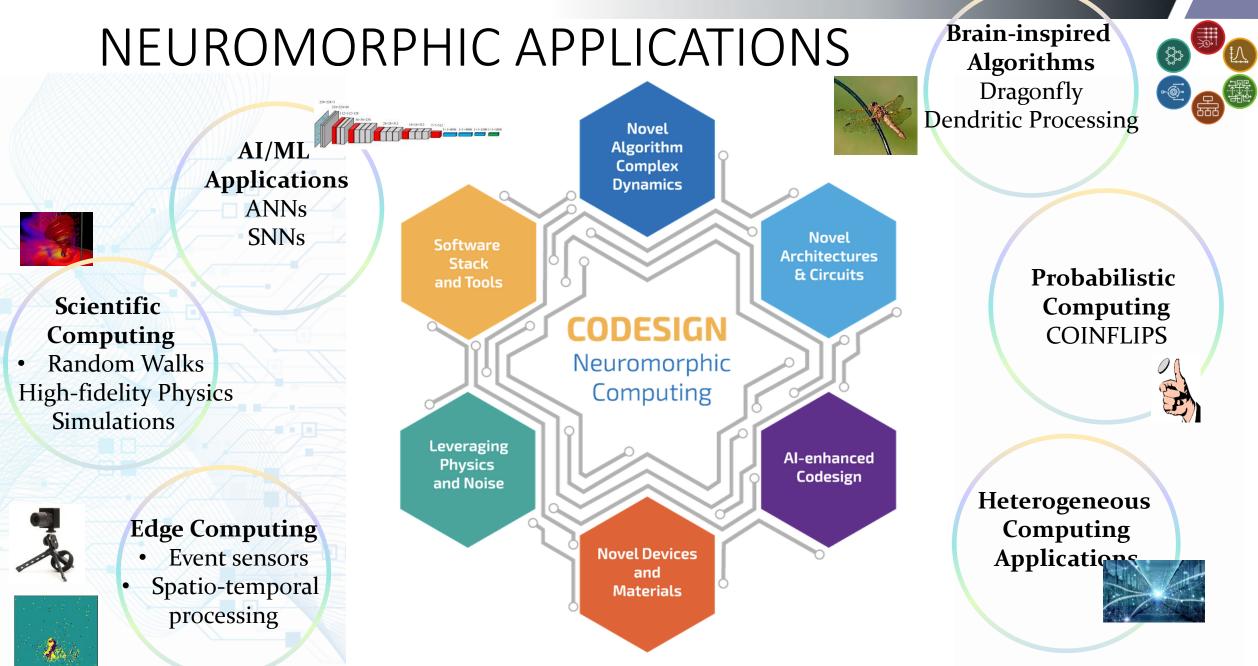
NEUROMORPHIC COMPUTING CHALLENGE SCALABILITY VS. COMPLEXITY



Hardware aware algorithms are critical for AI

- Novel neuroscience information translated to algorithms and models will influence next-generation devices, architectures
- Novel Algorithms
- Novel Devices
- Increased connectivity and communication (3D, wafer-scale, photonics)?

Scalability (# of Neurons, Synapses)



GOING FORWARD

Finally, policymakers should take proactive steps to ensure that researchers with small or moderate budgets can effectively contribute to the AI research field.

Concentrating

state-of-the-art technologies among the small number of research centers possessing extremely large compute budgets risks creating oligopolistic markets and shrinking the talent pool and opportunities for researchers.

The price of computations in gigaFLOPS has not decreased since 2017.15

price per computation

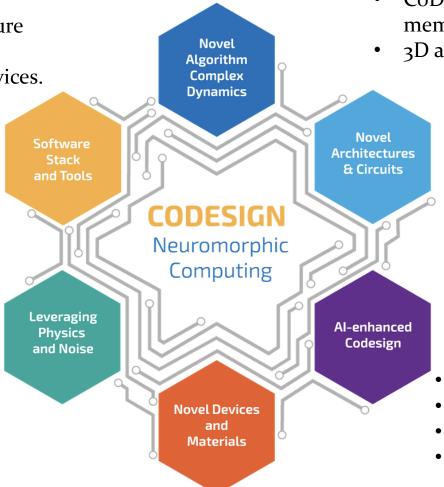
Limited direct neuromorphic investment even though it has been a more established field

Enable resources for research. Not just compute but training

Major overhauls of the computing paradigm like quantum computing or neuromorphic chips might one day allow for vast amounts of plentiful new compute.

LONG-TERM GOALS FOR NEXT-GENERATION OF **NEUROMORPHIC SYSTEMS**

- Algorithms are cognizant of architecture and device constraints.
- Leverage the complex dynamics of devices.
- Bio-inspired techniques, adoption in computing
- Software tools to support • design and development
- Integration with AI-enhanced techniques?
- Leverage the physics of devices to do computation (analog)
- Embrace stochasticity of devices ٠
- Analog devices are noisy. How can we incorporate this into algorithms?



- Heterogeneous architectures
- CoDesign to optimize communication and memory bottlenecks
- 3D architectures, Photonics
 - How can AI-enhanced techniques • accelerate scientific discovery?
 - Different AI techniques at the device, • circuit, system design and architecture level.
 - Enable encoding of domain ٠ knowledge
 - Enable concurrent contribution from researchers
 - Novel devices with complex dynamics
 - **Radiation-hardened devices** ٠
 - Reconfigurable devices ٠
 - Computational efficiency and computational density

THANK YOU!

References

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