From Atoms to Architecture :

The LBNL Beyond-CMOS Co-Design Program

LBNL Team : S. Griffin, L. W. Martin, L. Ramakrishnan, R. Ramesh (PI),
S. Salahuddin, P. Shafer, J. Shalf, D. Vasudevan, Z. Yao, & D. Armbrust

Technology Scaling Trends

Exascale in 2022… and then what?

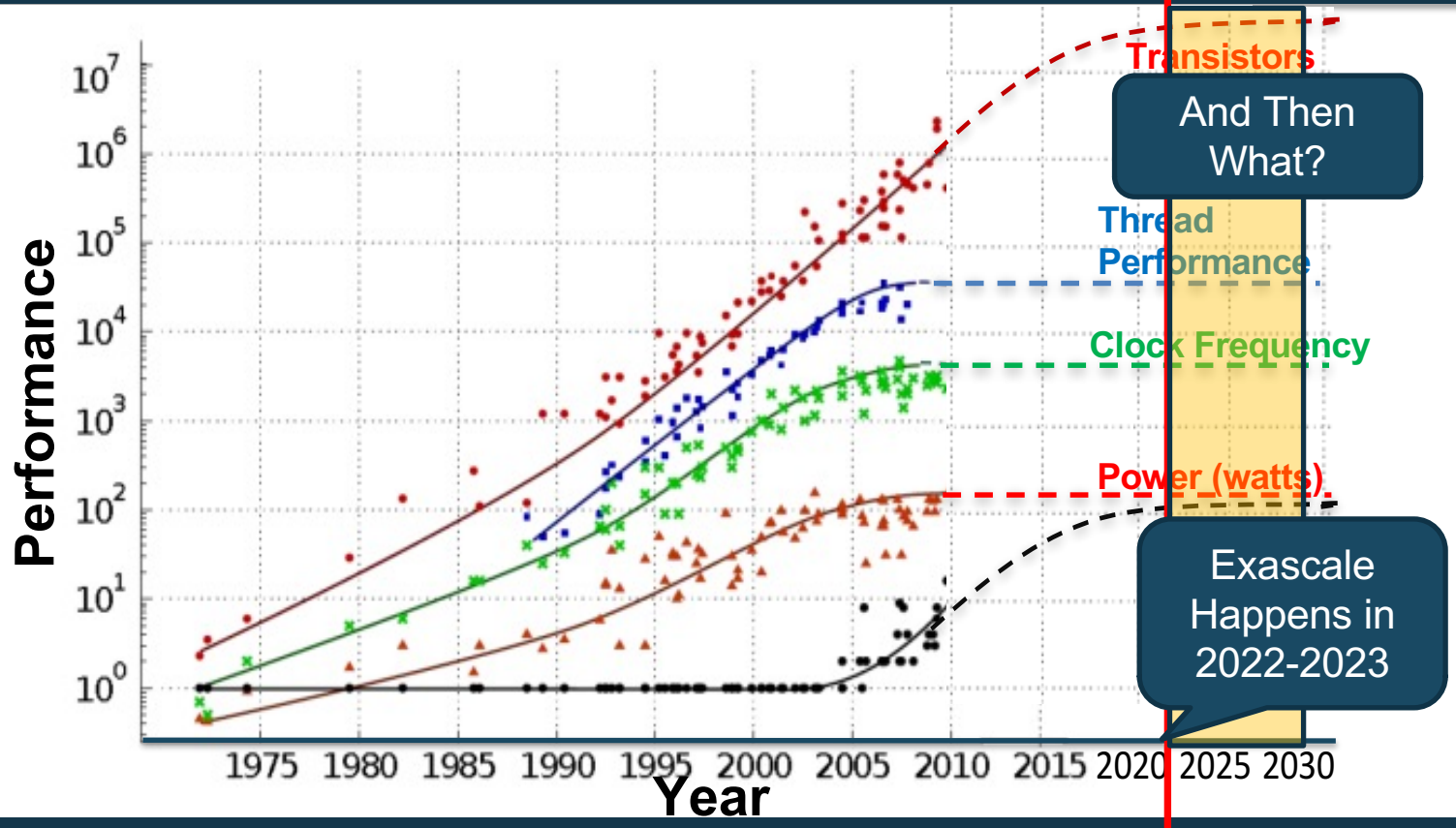
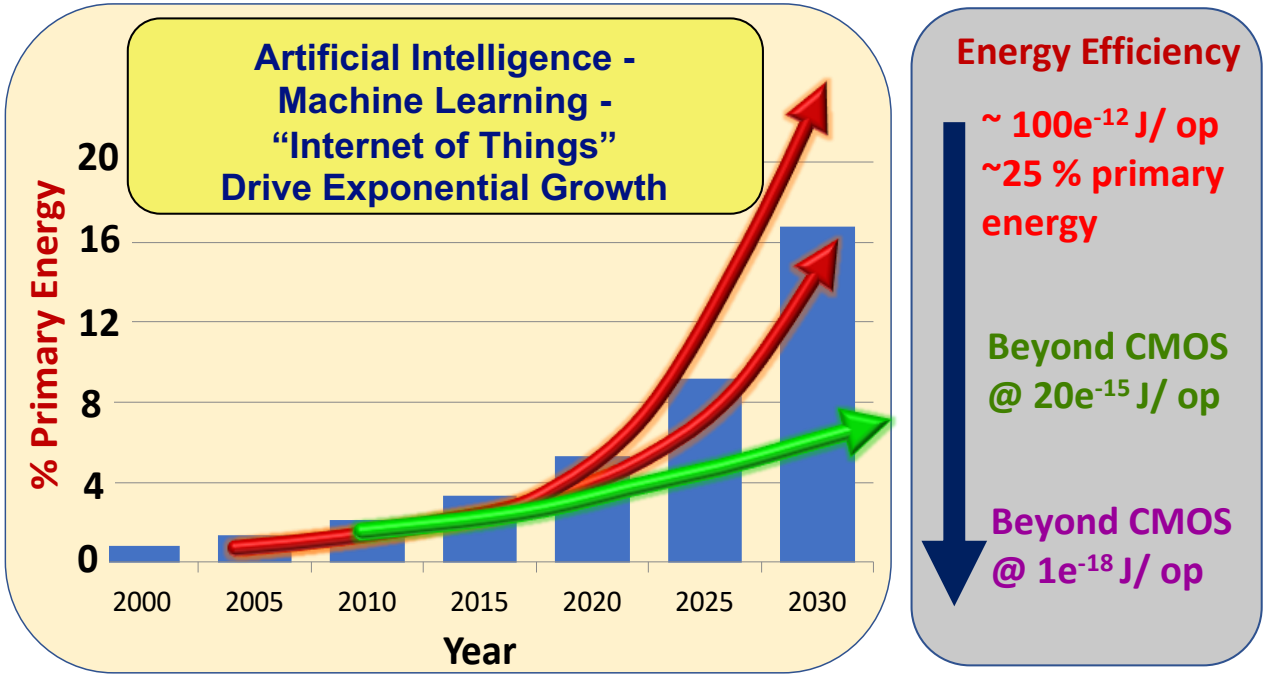


Figure courtesy of Kunle Olukotun, Lance Hammond, Herb Sutter, and Burton Smith

Beyond CMOS Electronics : Focus on Energy

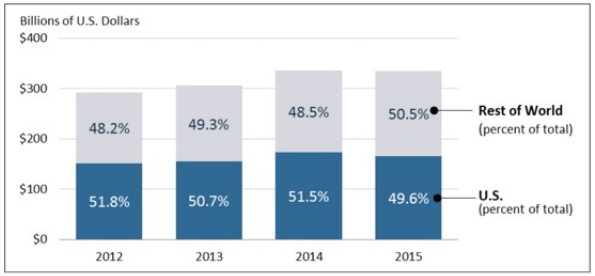
Microelectronics could get to ~25% of Primary Energy by 2030



Semiconductor Research Corporation
Decadal Plan for Semiconductors, 2020

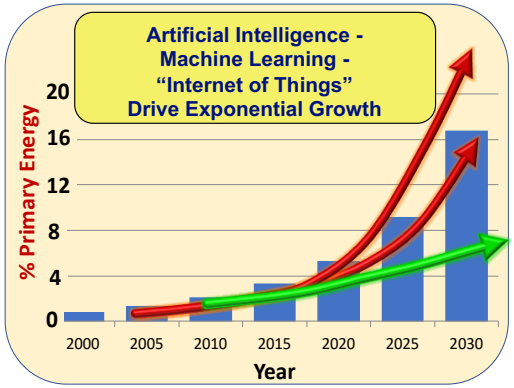
Global Drivers : The Challenge & The Opportunity

Global Competition & Market Share



Source: Semiconductor Industry Association (SIA), *The U.S. Semiconductor Industry, 2014, 2015, and 2016 Factbooks.*

China: $120B-$150B Investment



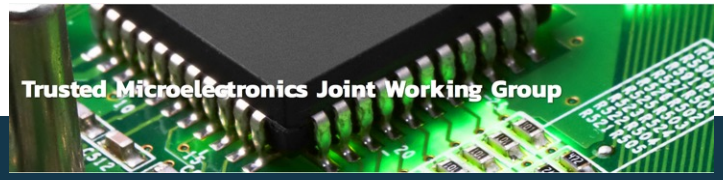
SRC Decadal Plan for Semiconductors, 2020

Energy Efficiency

- ~ $100e^{-12}$ J/ op
- ~25 % primary energy
- Beyond CMOS @ $20e^{-15}$ J/ op
- Beyond CMOS @ $1e^{-18}$ J/ op

National Security

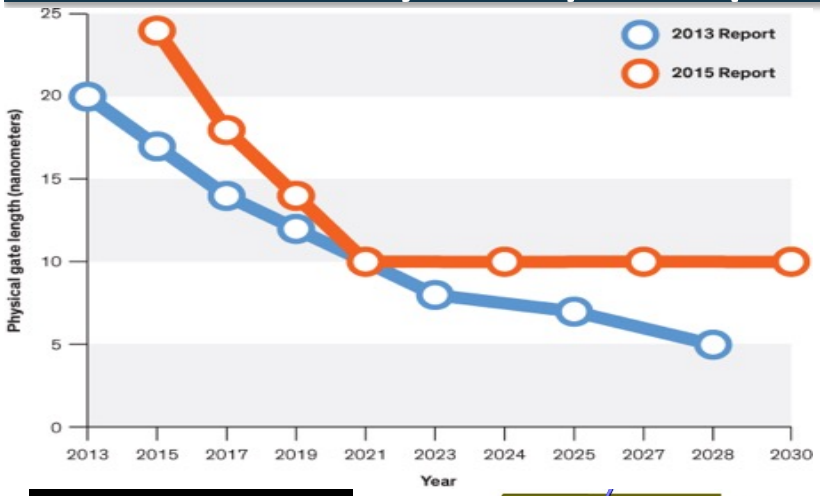
Energy Consumption

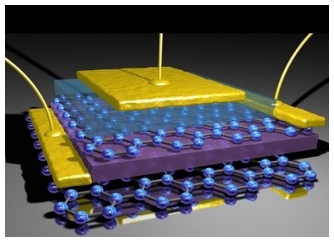


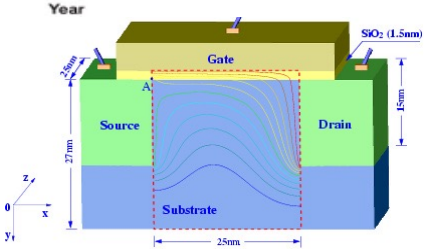
BERKELEY LAB

OSTP Report 2013-2015

Many *Incomplete* Options for New Device Technology (need codesign)







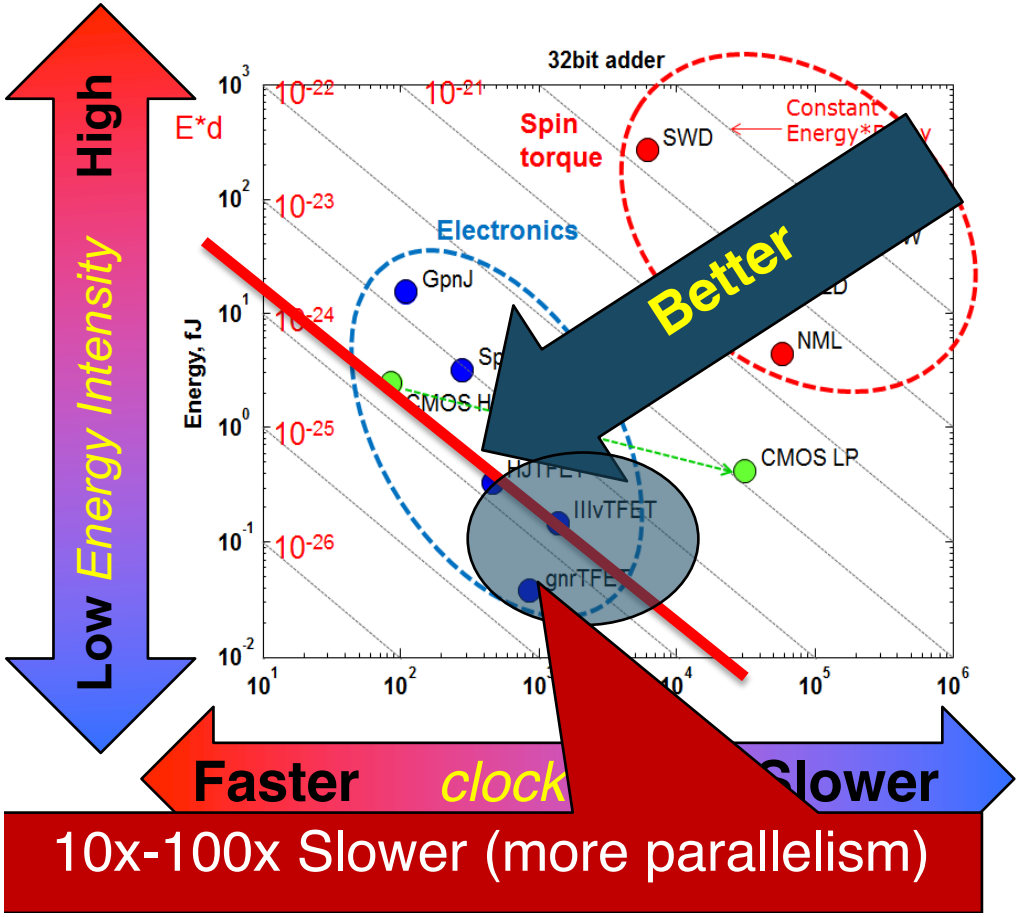
OSTP Report 2015: John Shalf
Robert Leland and Shekhar Borkar

TABLE 1. Summary of techology options for extending digital electronics.

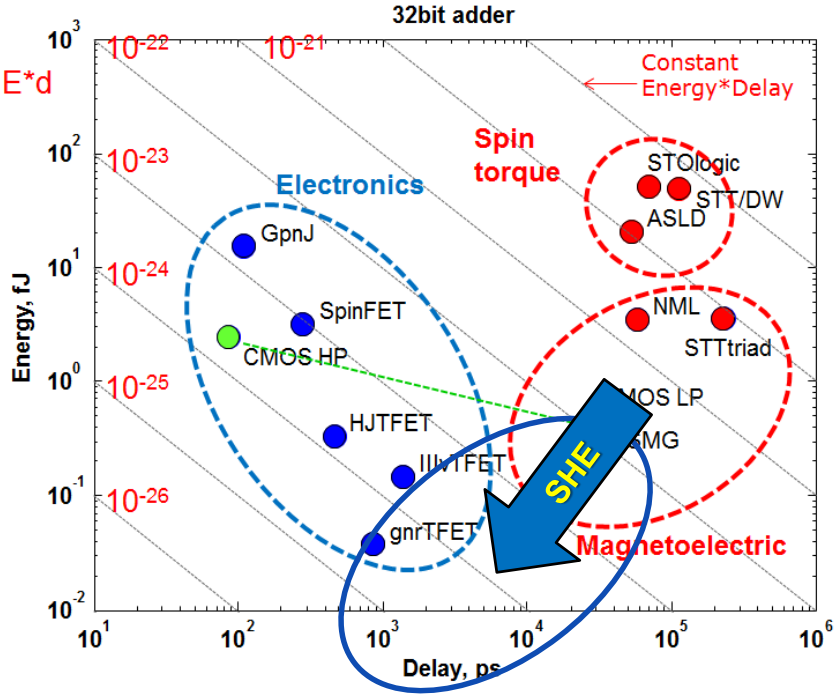
Improvement Class	Technology	Timescale	Complexity	Risk	Opportunity
Architecture and software advances	Advanced energy management	Near-Term	Medium	Low	Low
	Advanced circuit design	Near-Term	High	Low	Medium
	System-on-chip specialization	Near-Term	Low	Low	Medium
	Logic specialization/dark silicon	Mid-Term	High	High	High
	Near threshold voltage (NTV) operation	Near-Term	Medium	High	High
3D integration and packaging	Chip stacking in 3D using thru-silicon vias (TSVs)	Near-Term	Medium	Low	Medium
	Metal layers	Mid-Term	Medium	Medium	Medium
	Active layers (epitaxial or other)	Mid-Term	High	Medium	High
Resistance reduction	Superconductors	Far-Term	High	Medium	High
	Crystaline metals	Far-Term	Unknown	Low	Medium
Millivolt switches (a better transistor)	Tunnel field-effect transistors (TFETs)	Mid-Term	Medium	Medium	High
	Heterogeneous semiconductors/strained silicon	Mid-Term	Medium	Medium	Medium
	Carbon nanotubes and graphene	Far-Term	High	High	High
	Piezo-electric transistors (PFETs)	Far-Term	High	High	High
Beyond transistors (new logic paradigms)	Spintronics	Far-Term	Medium	High	High
	Topological insulators	Far-Term	Medium	High	High
	Nanophotonics	Near/Far-Term	Medium	Medium	High
	Biological and chemical computing	Far-Term	High	High	High

There are many options available, but Its hard to replace CMOS!

Nikonov & Young



Dramatic improvements with Codesign!

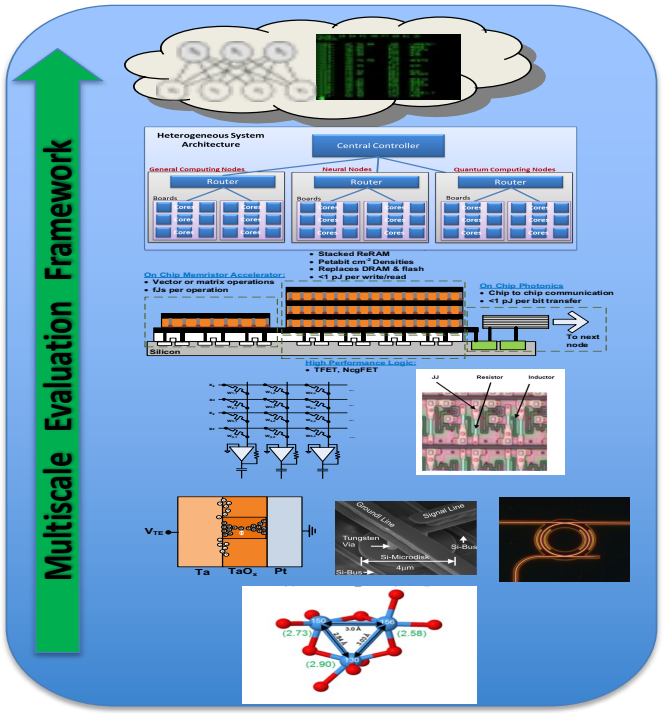


Just going from a single device (current practice) To a 32 bit adder yields huge improvements in Useful performance from the community

DOE Big Ideas Summit (BIS3) 2016

John Shalf (LBNL/Computing)
Rick McCormick (Sandia)
Ramamorthy Ramesh (LBNL/Energy Research)
Patrick Naulleau (LBNL / ALS / CXRO / EUREKA)

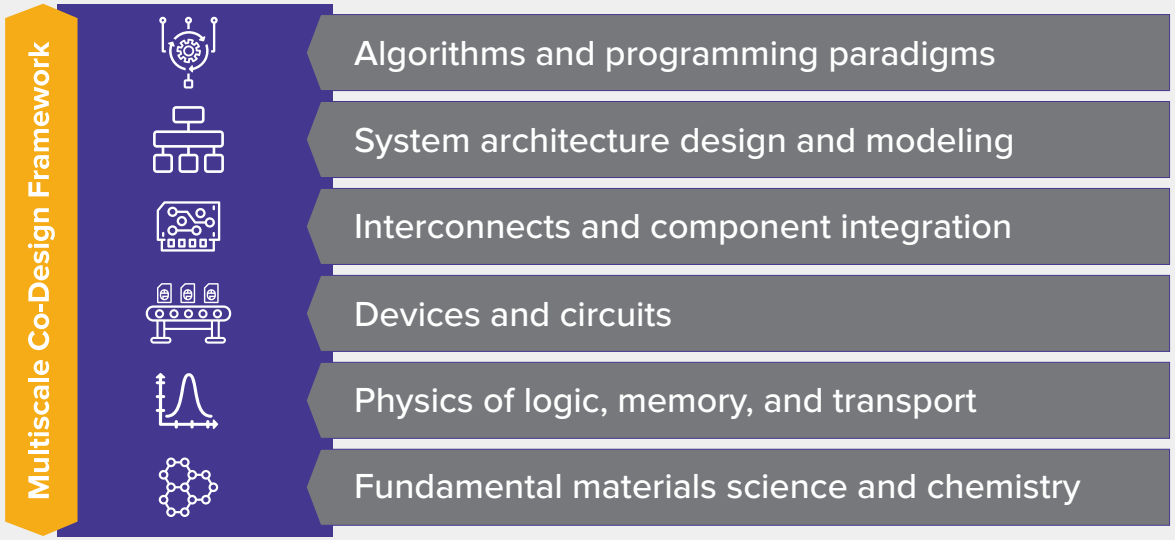
Multiscale Multi-Lab Effort



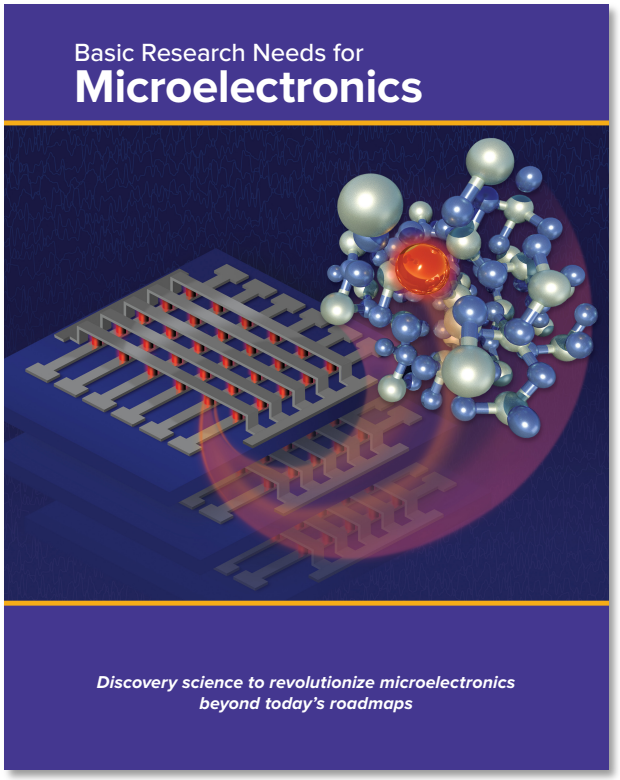
DOE Microelectronics BRN (BES, HEP, ASCR) 2018

We need to accelerate the pace of discovery by orders of magnitude

Deep Microelectronics CoDesign Framework



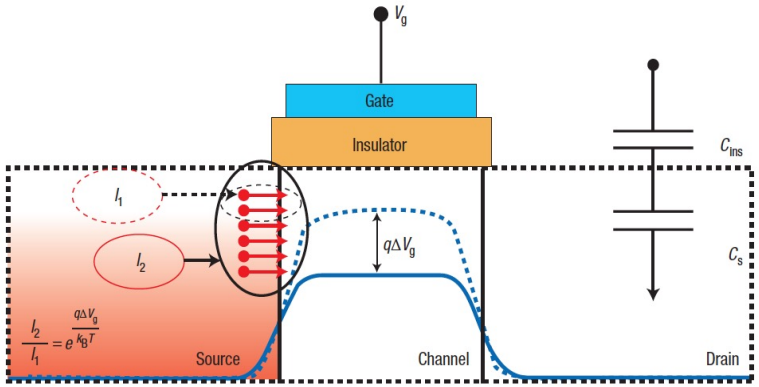
Co-design involves multi-disciplinary collaboration that takes into account the interdependencies among materials discovery, device physics, architectures, and the software stack for developing information processing systems of the future. Such systems will address future DOE needs in computing, power grid management, and science facility workloads.



Need a fundamental paradigm shift

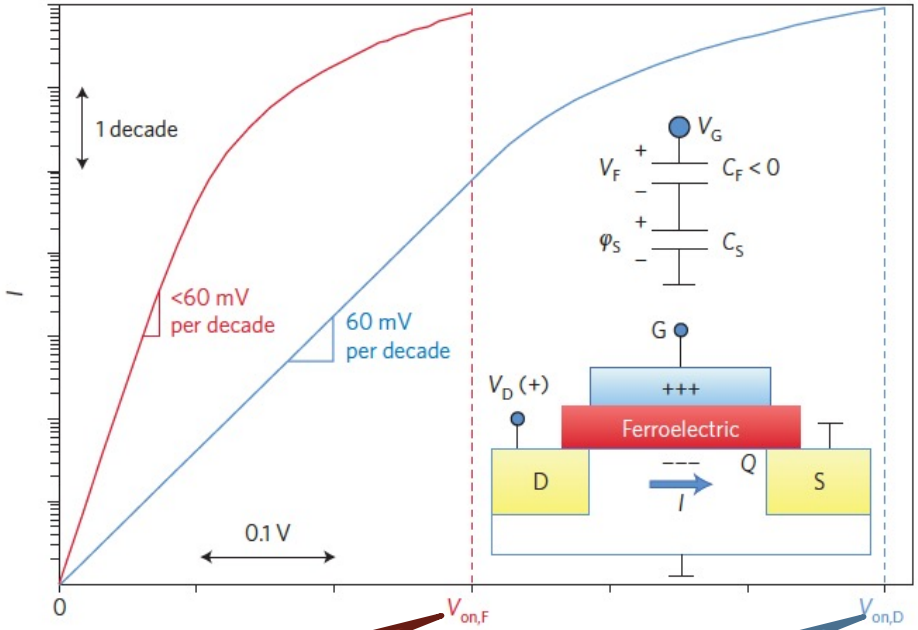
From Boltzmann Tyranny to Correlations

$$F(\text{state}) \propto e^{-\frac{E}{kT}}$$



$$\mathbf{I} \; \boldsymbol{\alpha} \; \exp(qV_g/k_BT)$$

$$k_BT\ln 10/q = 60 \text{ mV}$$



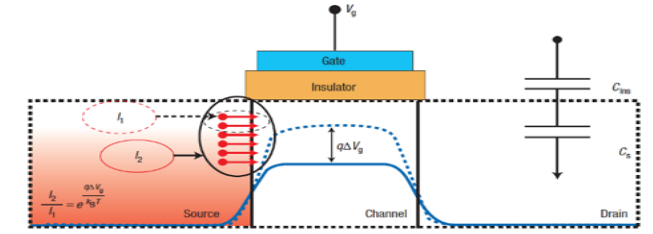
NCFET 90mV

MOSFET 0.7-0.5V

BERKELEY LAB

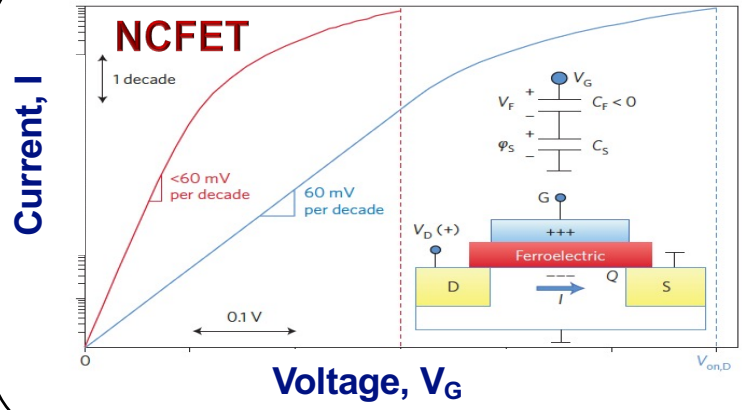
From Boltzmann "Tyranny" to Quantum Materials

$$F(\text{state}) \propto e^{-\frac{E}{kT}}$$



$$\mathbf{I} \; \boldsymbol{\alpha} \; \exp(qV_g/k_BT)$$

$$k_BT\ln 10/q = 60 \text{ mV}$$



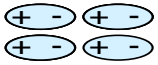
Ferromagnetism
Spontaneous Magnetization

Spin

Ferroelasticity
Spontaneous Strain

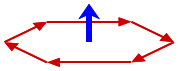
Phonon

Ferroelectricity
Spontaneous Polarization



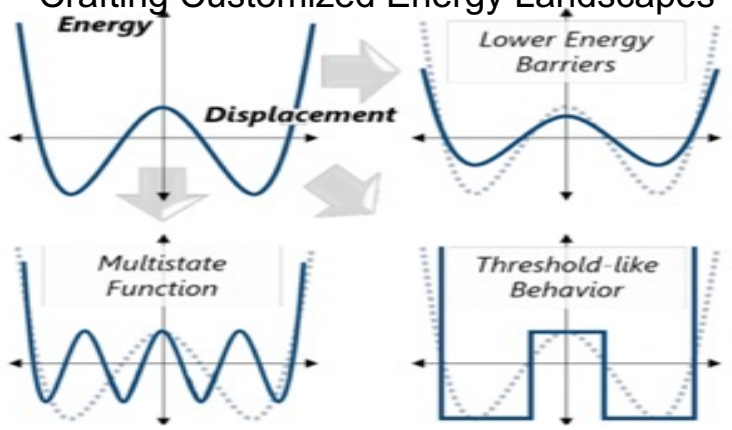
Charge

Ferrotorodicity
Spontaneous Toroidal Moment

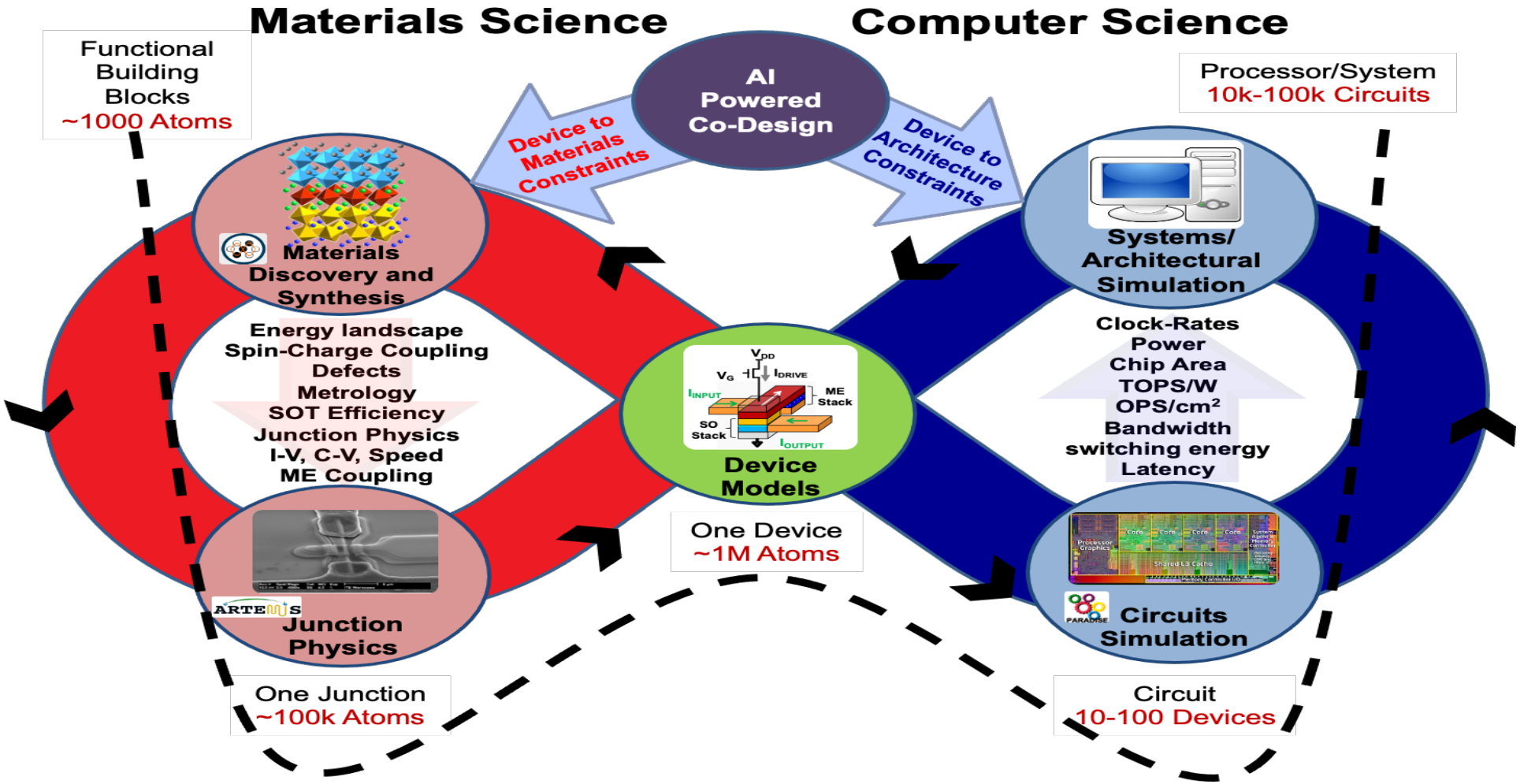


Spin/Charge

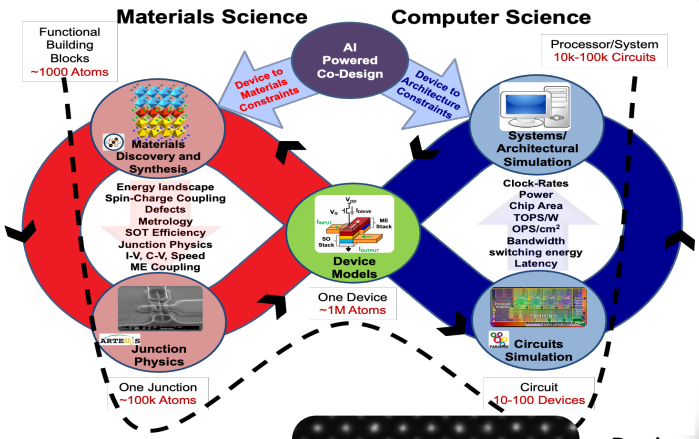
Crafting Customized Energy Landscapes

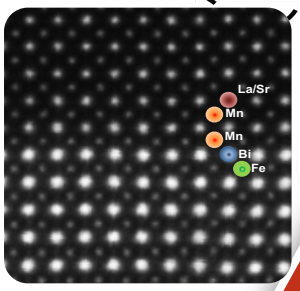


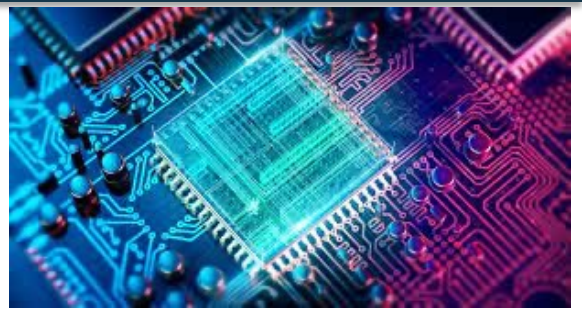
Co-Design From Atoms to Architecture

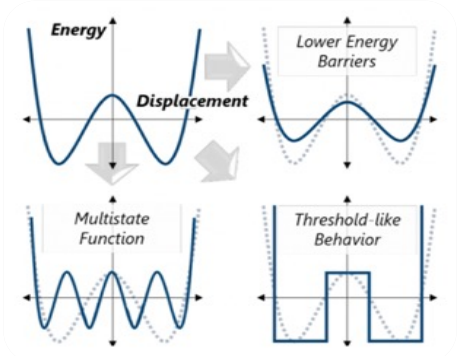


Co-Design From Atoms to Architecture



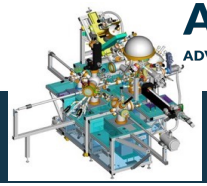






MATERIALS PROJECT

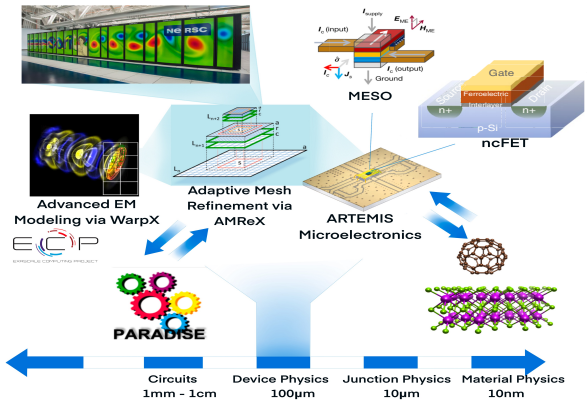
ALS ADVANCED LIGHT SOURCE

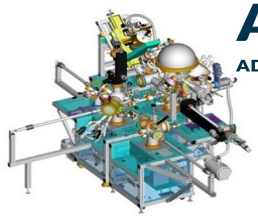


BERKELEY LAB

Leveraging the Power of DOE User Facilities

Co-design and CoSimulation defines materials requirements for NCFET & MESO devices

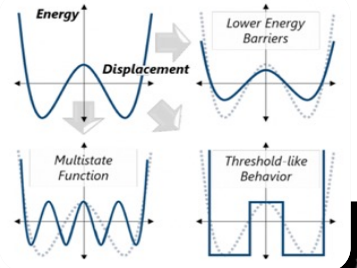




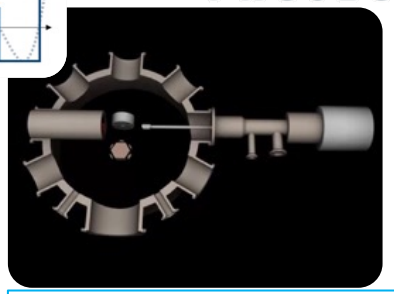
ALS
ADVANCED LIGHT SOURCE

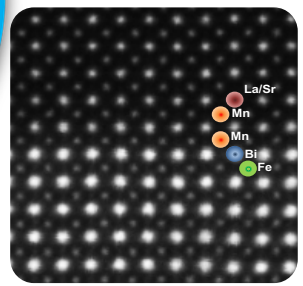
Probe limits of materials phenomena for logic-in-memory & NCFET's with goals of 100 mV, 10 ps, 1 aJ

Materials computation / simulation designs new materials and **energy- landscapes**



MATERIALS PROJECT





Precision synthesis of model materials systems

MOLECULAR FOUNDRY

Energy, spatial, and temporal probes explore ***multiferroic*** and ***ferroelectric*** materials phenomena

BERKELEY LAB

LBNL Beyond Moore Microelectronics Modeling and Simulation Framework

Accomplishment: Multidisciplinary effort developed end-to-end modeling framework to accelerate the microelectronic materials discovery process

Methods: Link-together computational models at different levels of scale to create multi-scale modeling framework for microelectronics.

Impact: Quantify impact of materials and device level advances in context of system-scale performance.

Provides quantitative and actionable feedback to direct future microelectronic materials and develop development

Device level & materials advances must be understood at the "systems" level and require an end-to-end process. Provides an accelerated Feedback path to focus device and Material Discovery Process

Application performance, System power → Switch speed, Power, Area, Fan-out, Stability → Interface-level, Losses/Performance → Materials metrics

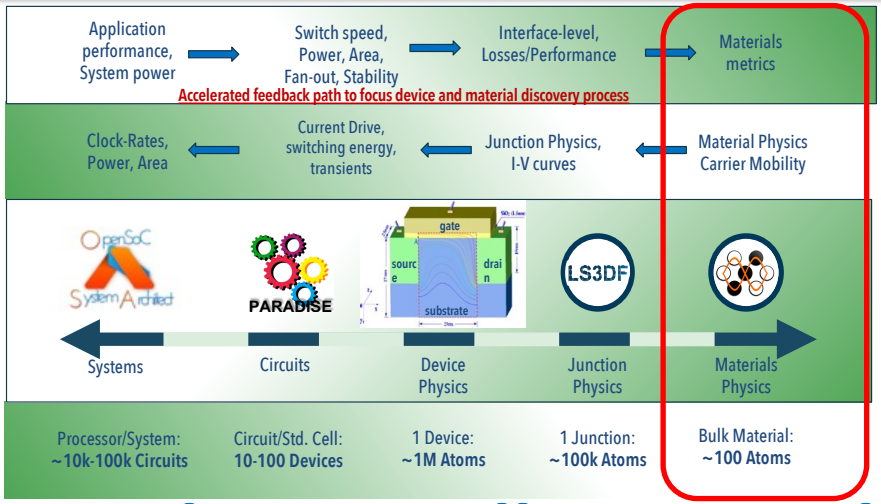
Accelerated feedback path to focus device and material discovery process

Clock-Rates, Power, Area ← Current Drive, switching energy, transients ← Junction Physics, I-V curves ← Material Physics Carrier Mobility

Systems | Circuits | Device Physics | Junction Physics | Materials Physics

Processor/System:	Circuit/Std. Cell:	1 Device:	1 Junction:	Bulk Material:
~10k-100k Circuits	10-100 Devices	~1M Atoms	~100k Atoms	~100 Atoms

BERKELEY LAB



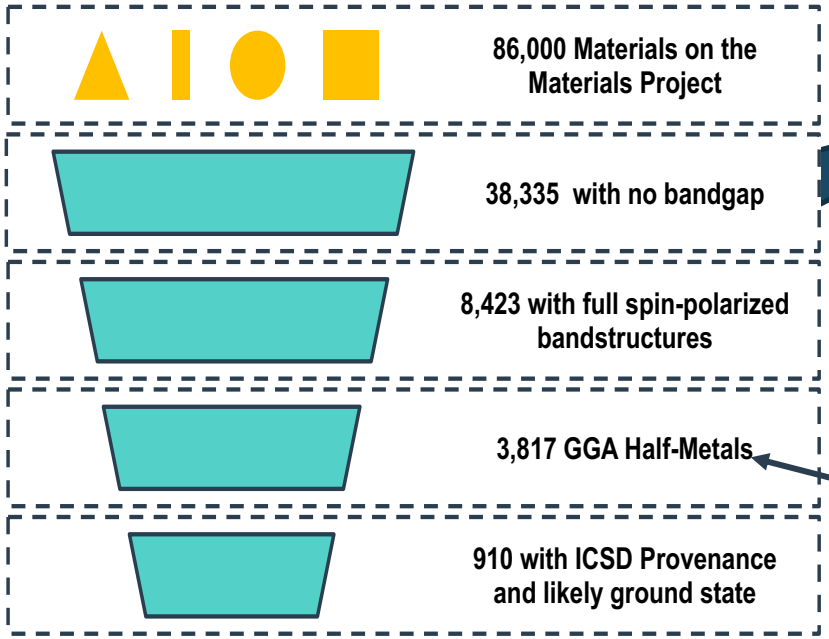
MATERIALS PROJECT

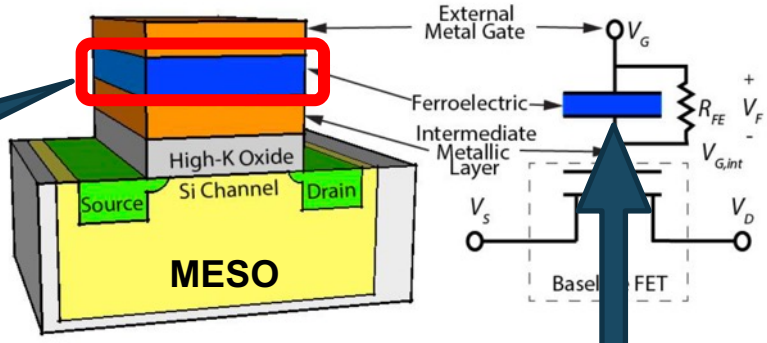
Simulating Bulk Materials

Identifying new candidate microelectronic materials from first-principles simulation.

MatProj Example:

Finding a Better Ferroelectric for MESO Devices



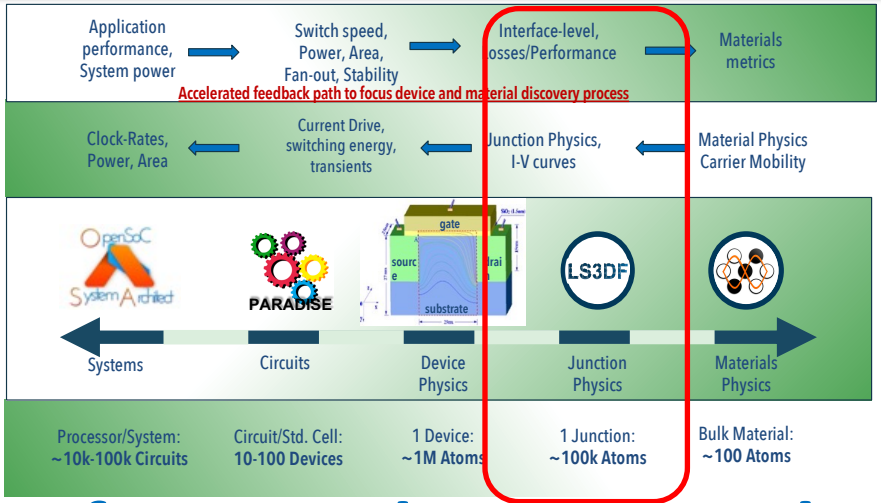


Conducting on one Spin Channel

Insulating on the other Spin Channel

Over 140 Potential Half-Metals for Experimental Investigation

Sinead Griffin



Interfaces and Junction Physics

"The Interface is the Device"

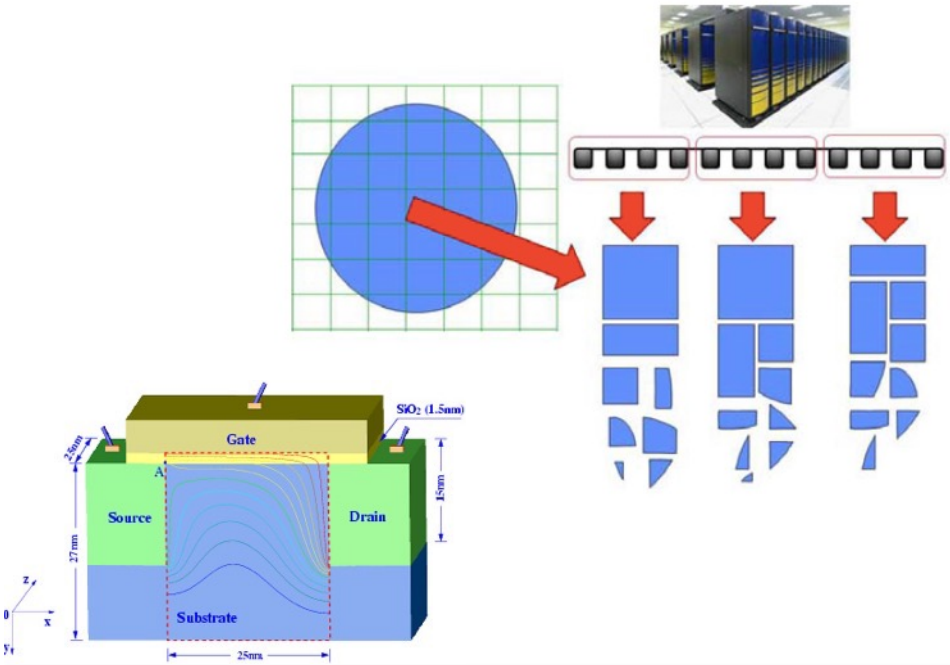
-Nobel laureate Herbert Kroemer

Ab-Initio Full Electronic Device Simulations

Scalable O(N) DFT Methods

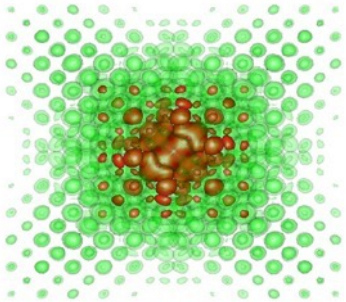
Sinead Griffin

Novel O(N) Problem Decomposition enables
Scalable modeling of emerging Post-Moore devices
Using First-Principles electronic structure calculations

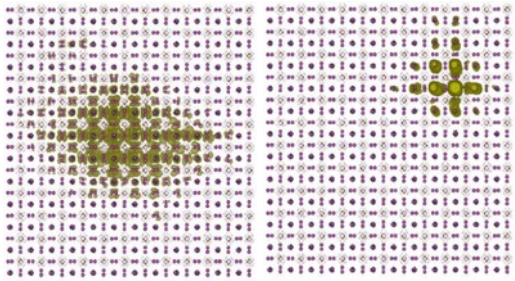


Accomplishments for BML

- Combined several techniques for a holistic, ab-initio, atomistic (beyond TCAD) device simulation
- LS3DF Device-size self-consistent ab initio calculations to get atomistic potential profile, band alignment, based boundary conditioned Poisson solver
- Based on the potential profile, and scattering state calculations to simulate the device transport, and leakage current etc.
- Using electron-phonon coupling to calculate the heat generation and dissipation at atomic scale



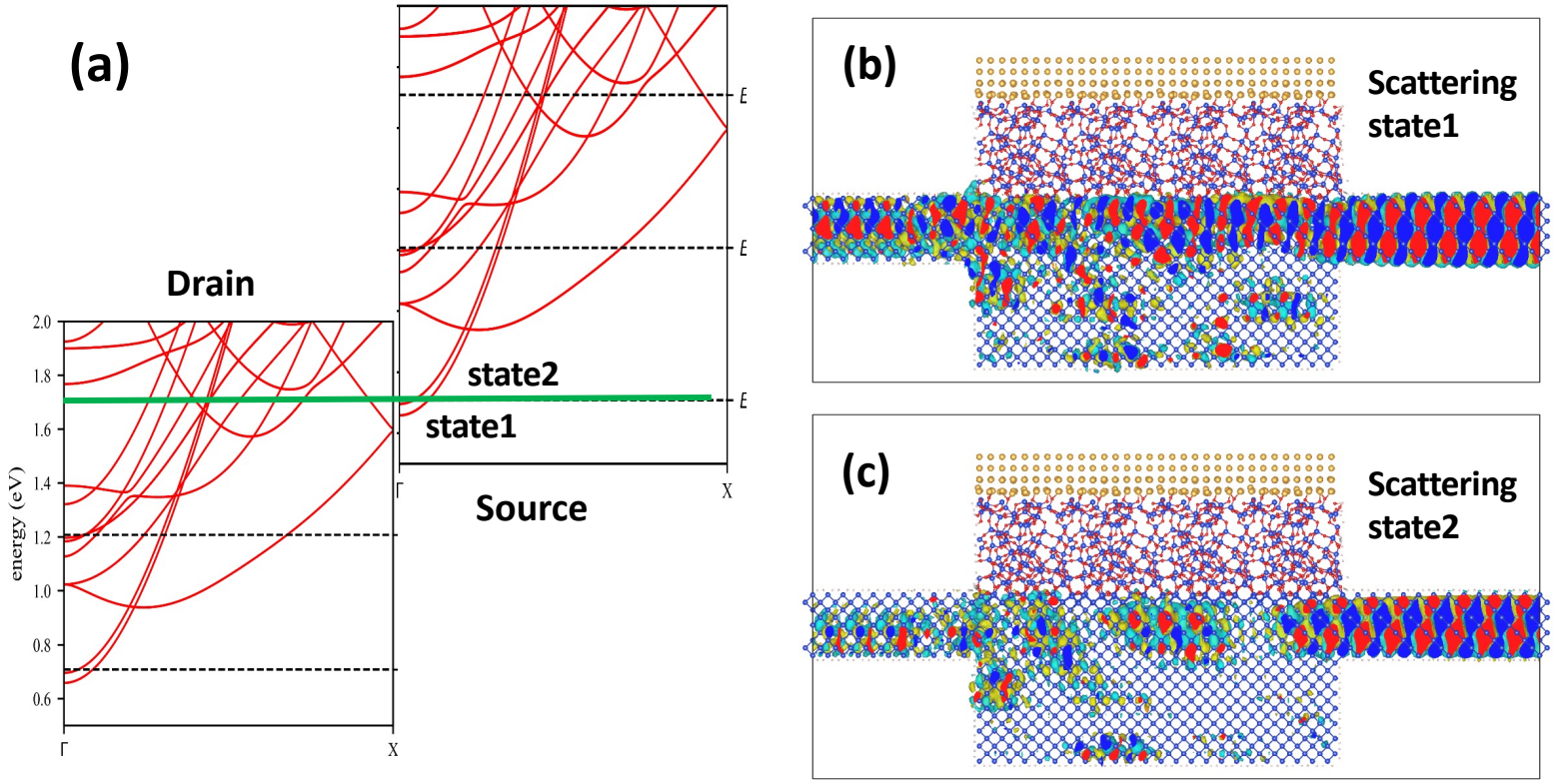
A shallow defect state in Si.

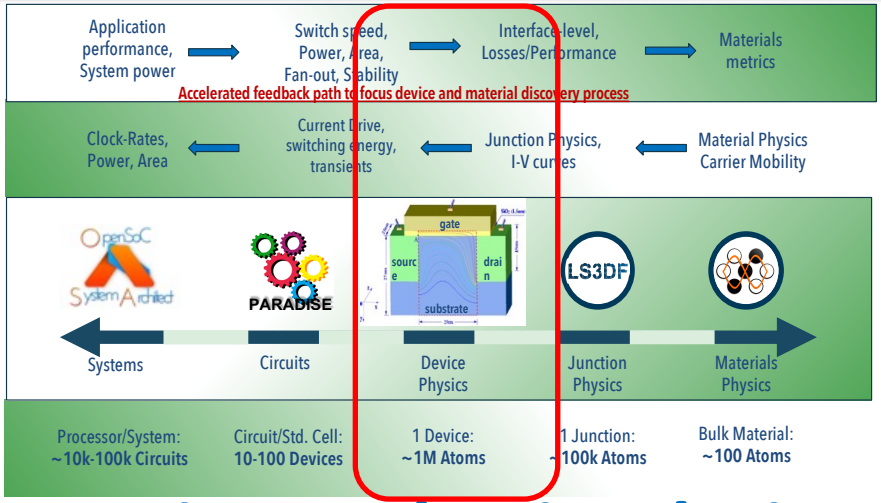


the electron (left) and hole (right) localizations in a bulk $CH_3NH_3PbI_3$ material. The small dots are atoms.

Simulate full device-scale interfaces

Sinead Griffin





Device Scale Simulation

ARTEMIS

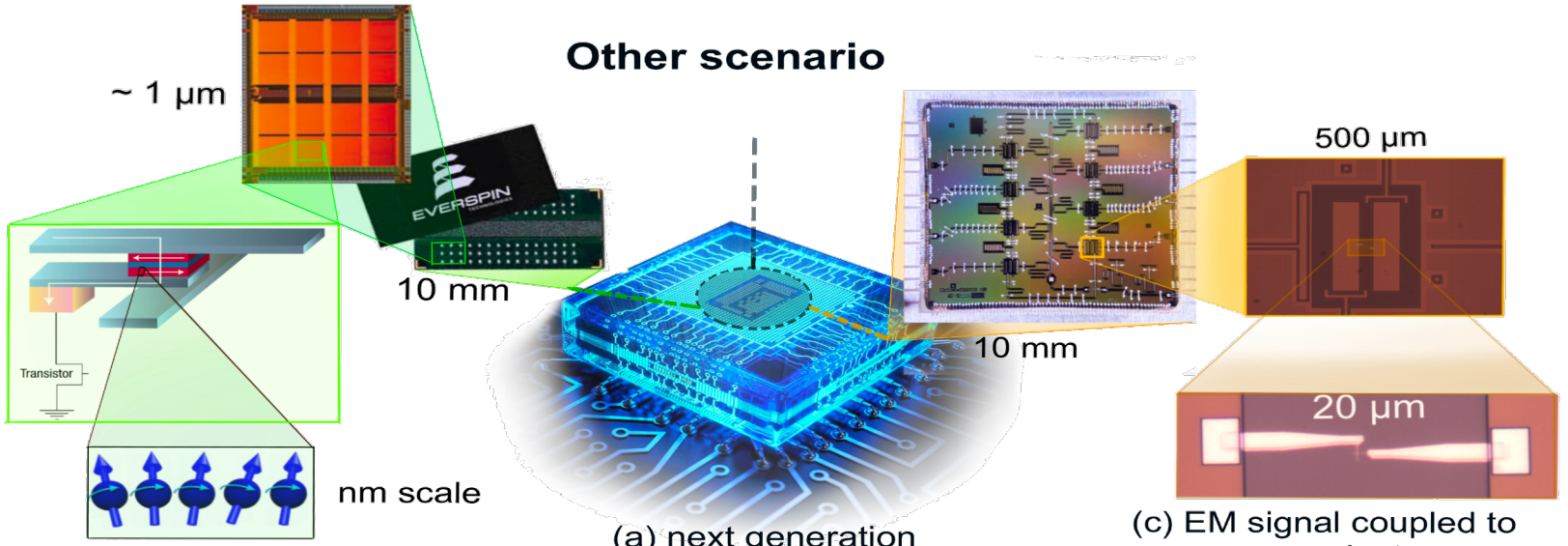
ECP ARTEMIS : Adaptive Mesh Refinement for Time-domain ElectrodynaMIcs Solver

Device-Scale Simulation using AMReX+Physical PDEs

ARTEMIS : Adaptive Mesh Refinement for Time-domain ElectrodynaMIcs Solver

Challenge: Wide range of physical coupling dimensions **from nm scale to cm scale**

- All types of physics talk to each other due to natural **nonlinearity** of spin oscillations, etc.



(b) EM signal coupled to magnetic spin: Magnetic random access memory (MRAM)

(a) next generation electronic circuitry with new devices launched on

(c) EM signal coupled to superconductors: Quantum chip

Solution Adaptive Mesh Refinement (AMR) simulation to cover length & time scales:

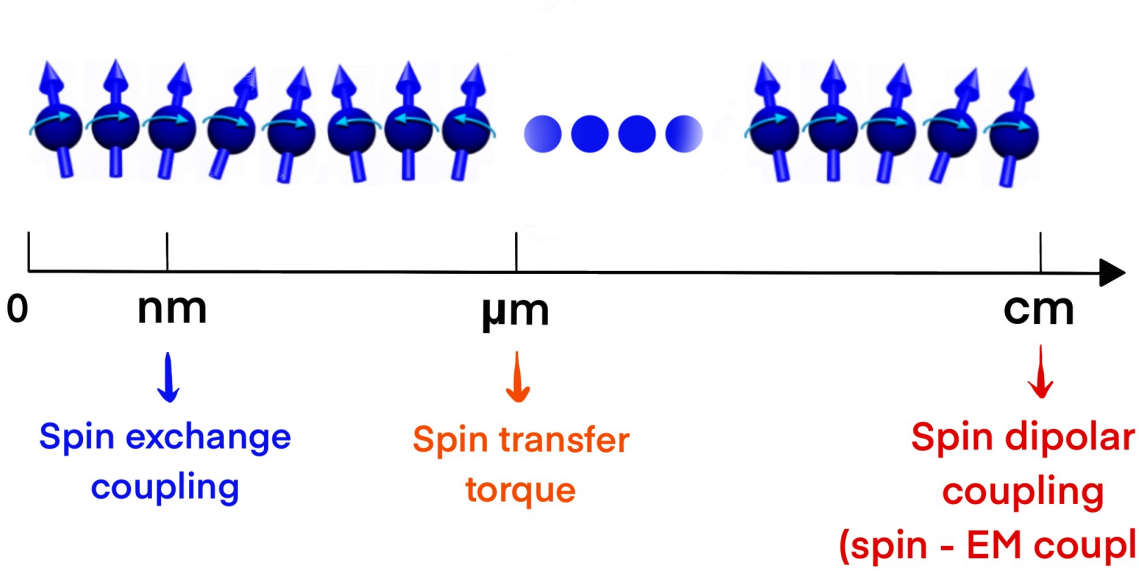
- Simultaneously solving the **coupled PDEs**, e.g. Maxwell's equations, LLG equations, etc.
- Adjust mesh resolution with **AMR** to the needs of specific physics in a specific region

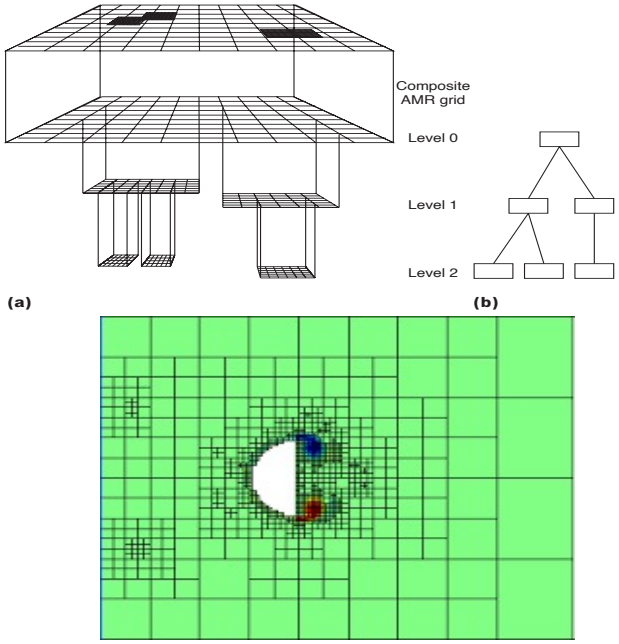
Device-Scale Simulation using AMReX+Physical PDEs

Jackie Yao and Andy Nonaka: LBNL Applied Math / CS

Challenge: Wide range of physical coupling dimensions **from nm scale to cm scale**

- All types of physics talk to each other due to natural **nonlinearity** of spin oscillations, etc.



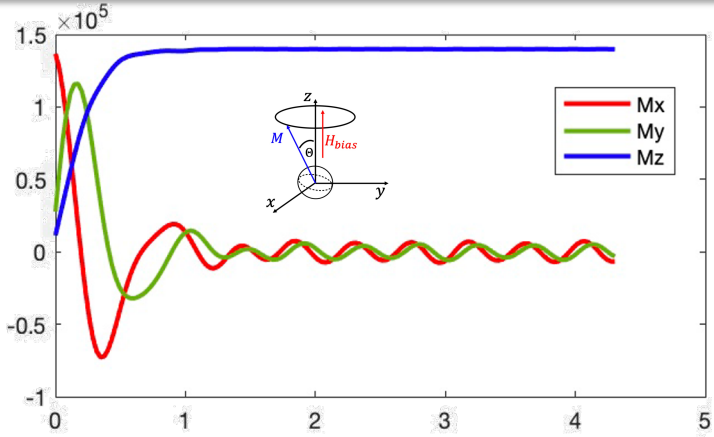


Solution Adaptive Mesh Refinement (AMR) simulation to cover length & time scales:

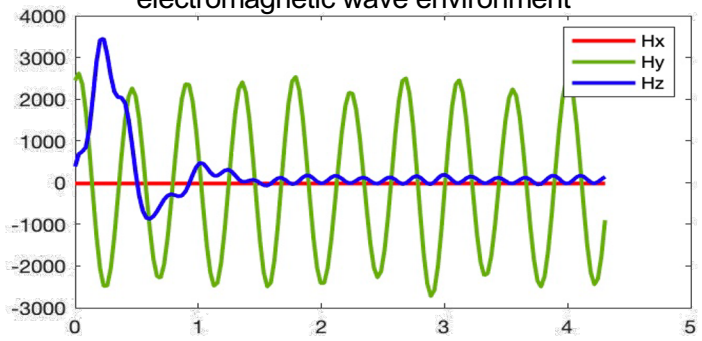
- Simultaneously solving the **coupled PDEs**, e.g. Maxwell's equations, LLG equations, etc.
- Adjust mesh resolution with **AMR** to the needs of specific physics in a specific region

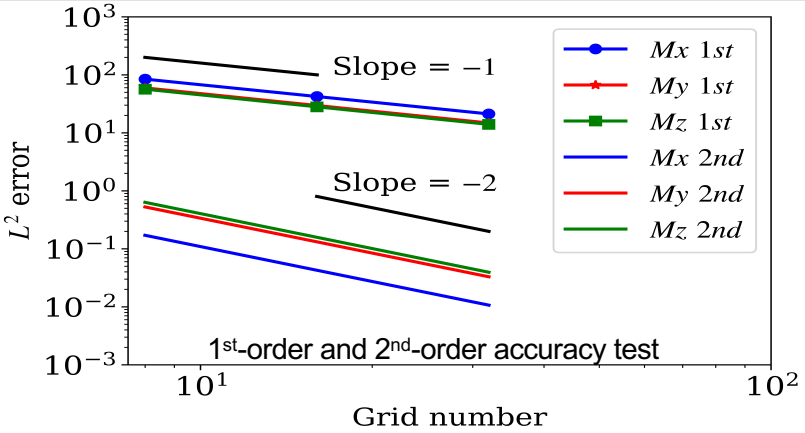
Early-stage Demonstration

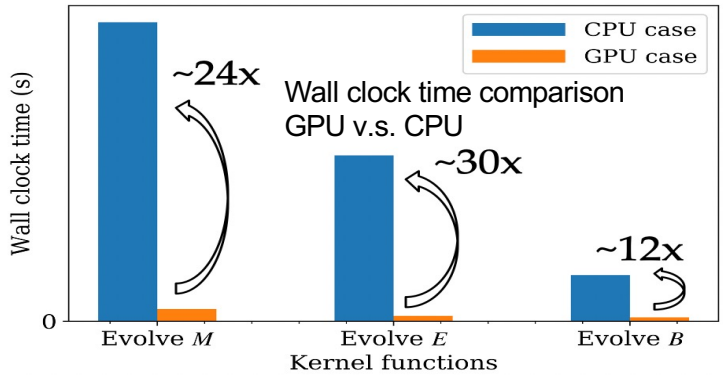
Jackie Yao and Ann Almgren: LBNL Applied Math / CS

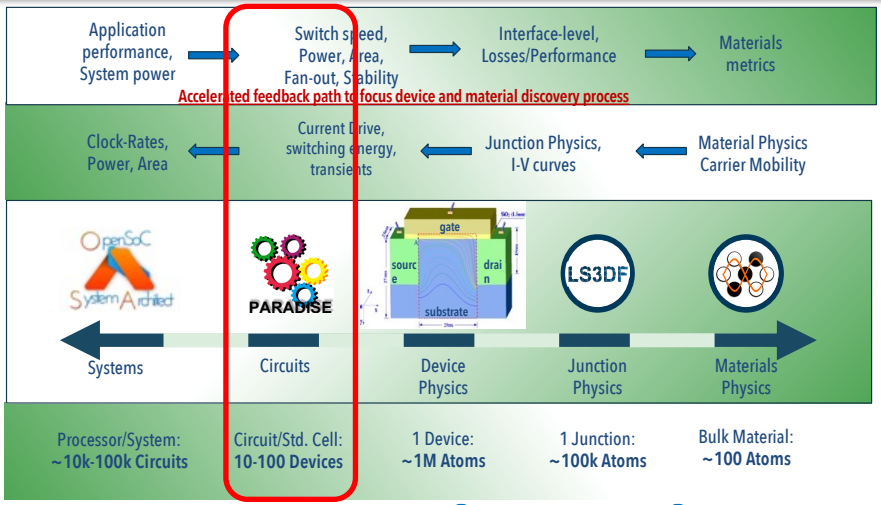


Single spin evolution in 2.4 GHz electromagnetic wave environment









Circuit Level Simulation

PARADISE: Post-Moore Architecture and Accelerator Design Space Exploration

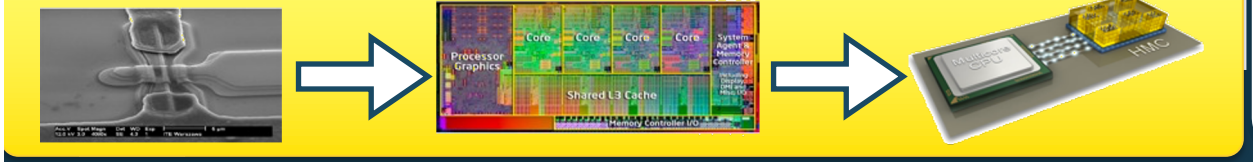
PARADISE: Post-Moore Architecture and Accelerator Design Space Exploration

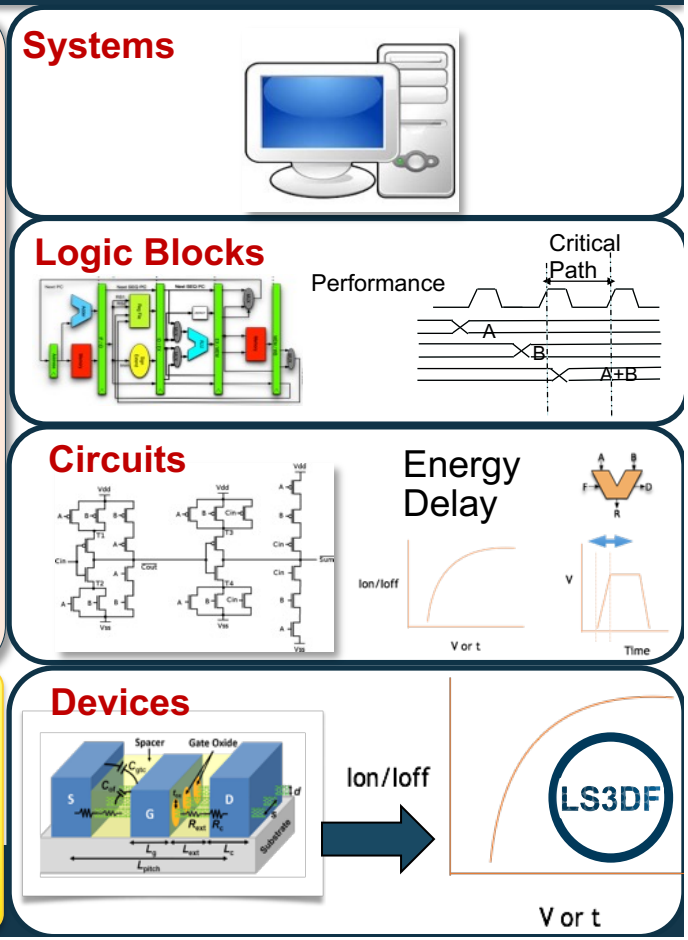
George Michelogiannakis, Dilip Vasudevan, John Shalf

- **Multiple devices, memories, and other "post Moore" technologies in development**
- **Evaluating each in isolation misses big picture**
  - Devices can be better designed with high-level metrics
  - Architects can evaluate how exploit new technologies

Until now, we lacked the tools to do so systematically and rapidly for many technologies

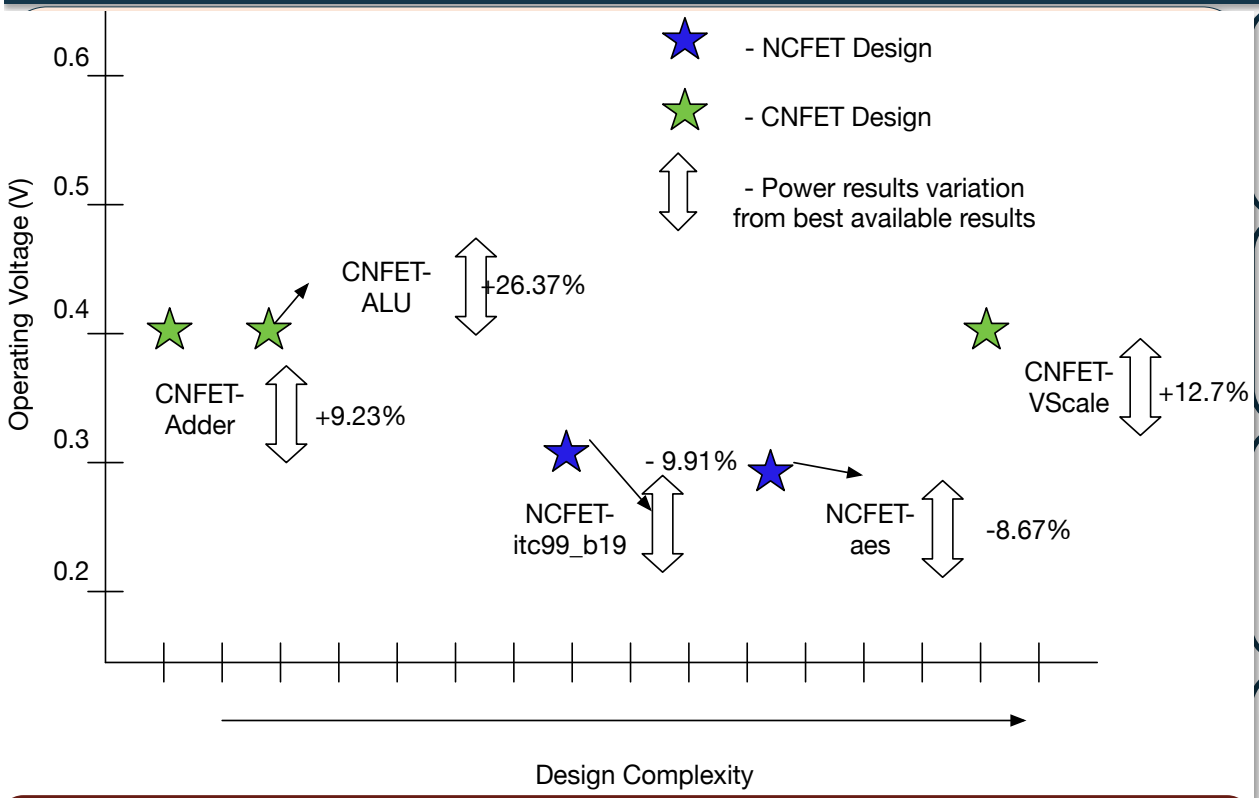
(PARADISE addresses that gap)





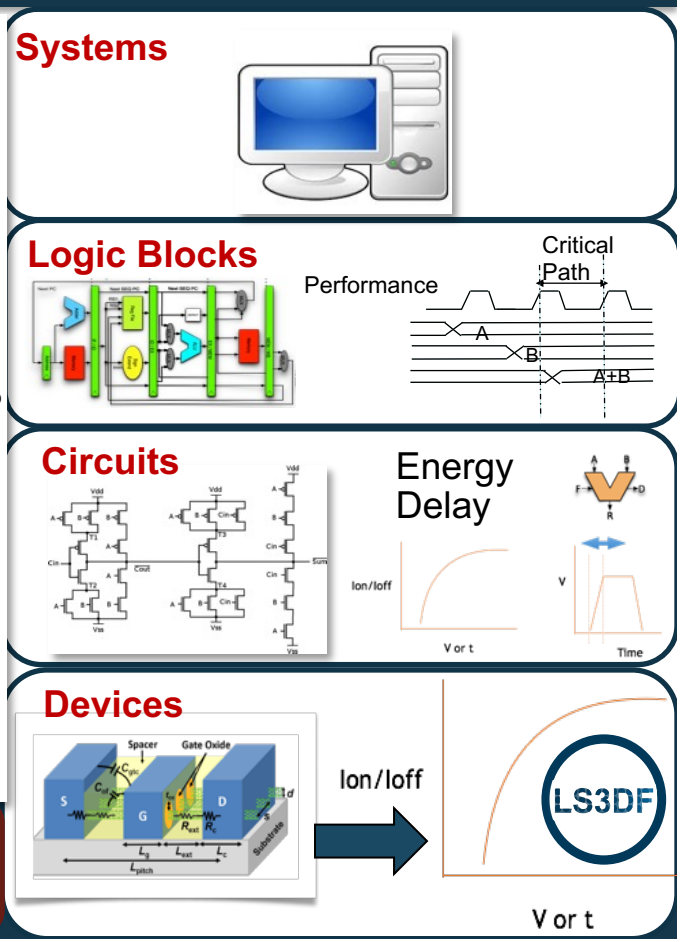
PARADISE: Post-Moore Architecture and Accelerator Design Space Exploration

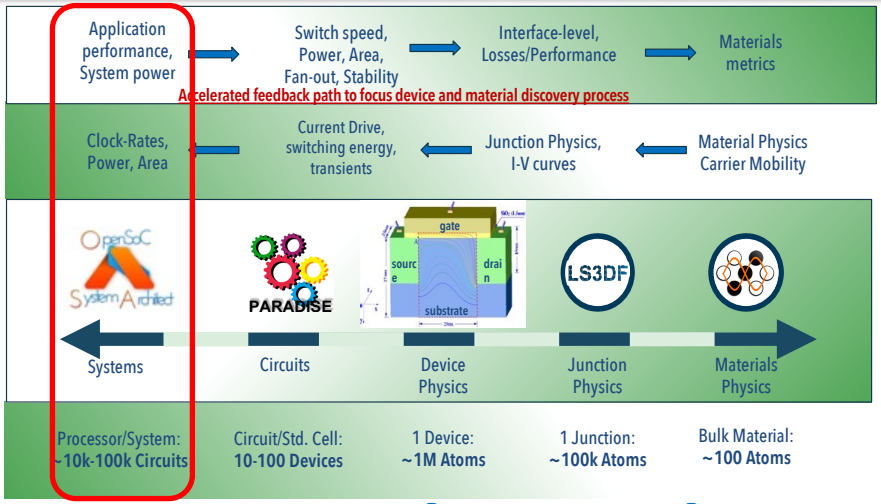
George Michelogiannakis, Dilip Vasudevan, John Shalf



PARADISE Accuracy Validated Against Experimental Results

Dilip P. Vasudevan, et. al.: PARADISE - Post-Moore Architecture and Accelerator Design Space Exploration Using Device Level Simulation and Experiments. ISPASS 2019: 139-140



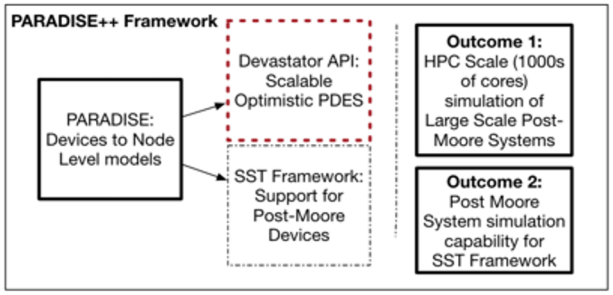


System Scale Simulation

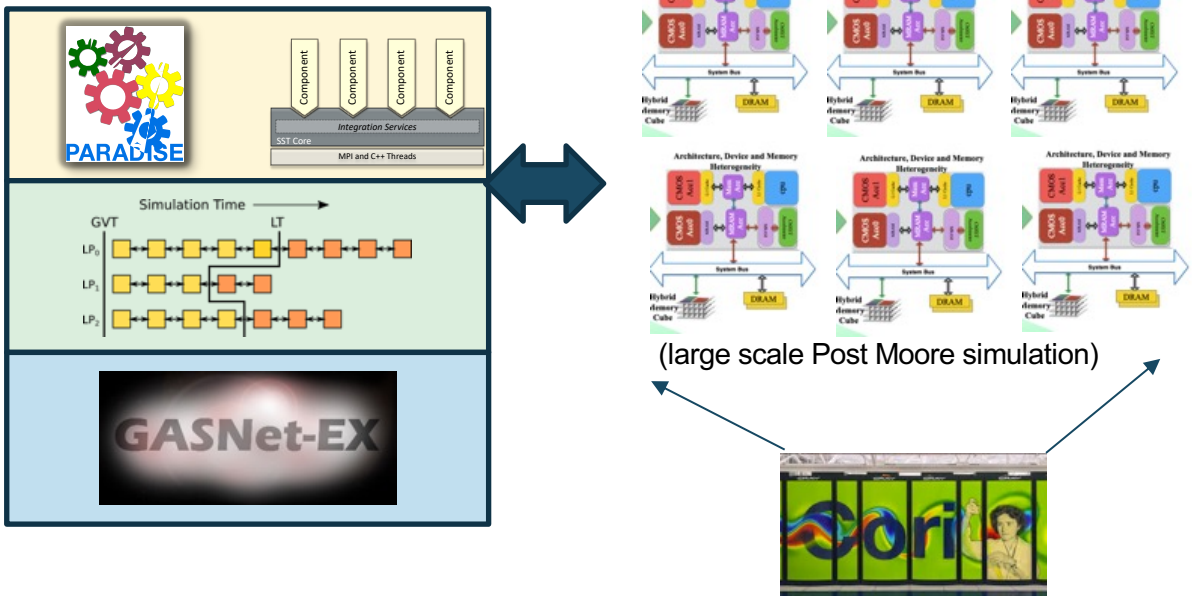
PARADISE++: Using Scalable Event-driven Optimistic Parallel Discrete Simulator for system-scale modeling

PARADISE++:

Large Scale Optimistic Synchronization based simulation of Post Moore Architectures

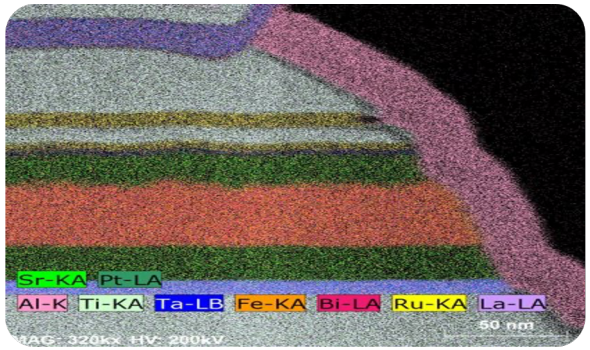


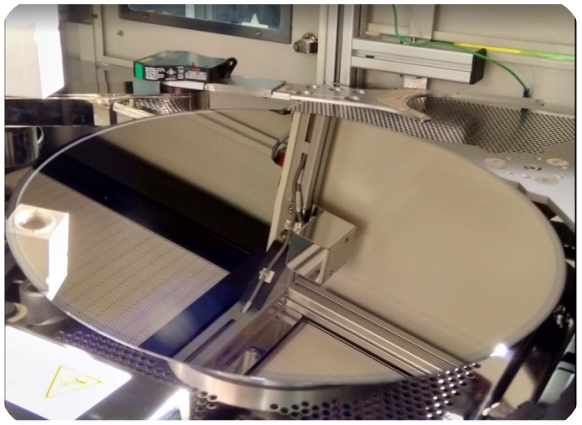
- Post Moore Device level to architectural level simulation support
- Optimistic Synchronization based PDES simulation
- SST extension for Post Moore Architectural support

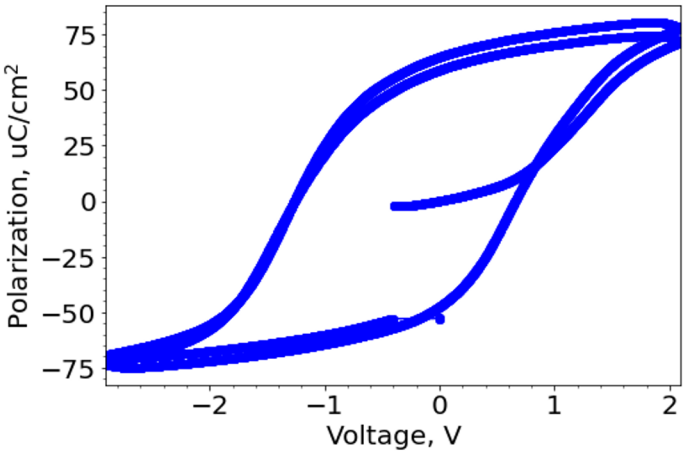


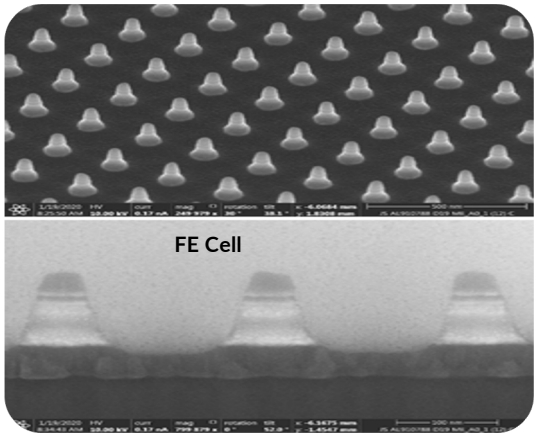
PARADISE++ simulation framework and its potential outcomes

Translating From Science to Technology : CMOS+X







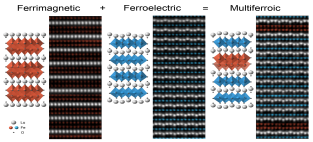
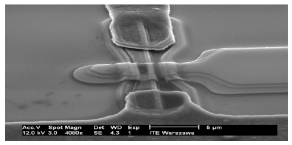
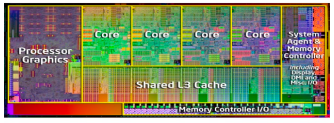
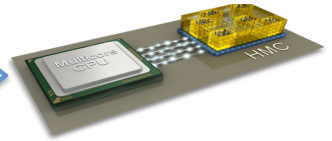


Key Points

Process integration of complex functional materials
Desperate need for US-based capabilities
Process control @ 1nm scale
200mm platform critical to demonstrate technology
Need for process modules: PVD, ALD, Etch, RIE

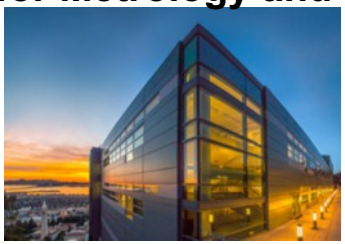
Leverage the Power of DOE's National User Facilities And Modeling Capability to Accelerate Microelectronics Discovery

End-to-End Acceleration of Discovery and Evaluation of New Devices

Materials Discovery	ME Transistor	Architecture	System
			
Computational Design Synthesis Characterization	Device Design Fabrication Parametrics	RTL/Gate Simulator Power Delay	Arch. Level Simulator TDP, EDP

National User Facilities for Metrology and Experimental Validation





ADVANCED LIGHT SOURCE

MOLECULAR FOUNDRY

NERSC National Energy Research Scientific Computing Center

Berkeley UNIVERSITY OF CALIFORNIA

EUREKA CXRO

Physical, Chemical, Materials and Computer Sciences

Next steps…

- **Do Great Team Science!! First papers are being prepared…**
- **BML Distinguished Lecture series on-going…**
- **Build collaborations across labs, industry academia**
- **Succeed with the "Co-Design" Mantra: the biggest learning for us!!**


Thank You