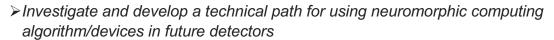
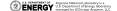


Applications: Future HEP/NP Detectors

- Very complex, large-scaled engineered devices
- Major challenge for data collection & analysis
- Future Circular Collider FCC-hh detector
 100s TB/s at 40 MHz bunch crossing
- Complex events, fast classification
- Requires real-time analysis at the sensors



➤ Investigate interconnect possibilities and develop design point requirements for future detectors





3

Detectors at Colliders: LHC Example

- Today:
 - Colliders L1 trigger latency (ASIC/FPGA) of 10 microsec, selecting 100K events/sec to the high-level trigger (CPU/GPU/FPGA), which selects about 1000 events
- Future:
 - Higher luminosity, bunching (temporal), more intelligent selection
 - With higher luminosity, pile-up challenges (multiple collisions per bunch crossing), both in-time and out-of-time
 - Power/speed requirements difficult with current technology extrapolations
 - Opportunities in more intelligent selection: pattern recognition, particle classification, more

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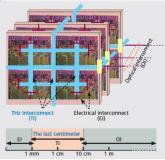
Materials Research

Neuromorphic Materials



- Focus on scaling down device parameters, critical to achieving low power operation
- Explore relationship between materials parameters and gate tunability of memtransistor synaptic response for learning

THz Interconnects



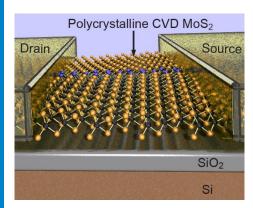
- Create frequency-agile wireless antennas to transmit and receive THz signals on a small footprint
- Focus on THz plasmonics

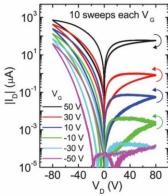
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5

Memtransistors Based on 2D Polycrystalline MoS₂





- Field-driven defect motion in 2D polycrystalline MoS₂ shows a 2-terminal memristive response
- Weak screening in atomically thin materials enables gate tunability like a transistor

Proposed Research:

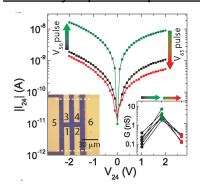
 Reduce device dimensions and operating voltage/power by controlling grain size and defect structure in 2D polycrystalline MoS₂ in addition to novel dielectrics (e.g., ferroelectrics) and contacts (e.g., THz plasmonics, topological semimetals)

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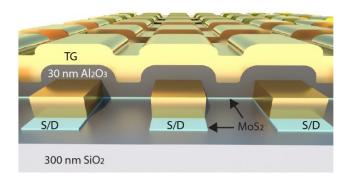


Multi-Terminal Memtransistors for Co-Design

Heterosynaptic Responses



<u>Dual-Gated Memtransistor Crossbar Arrays</u>



Proposed Research:

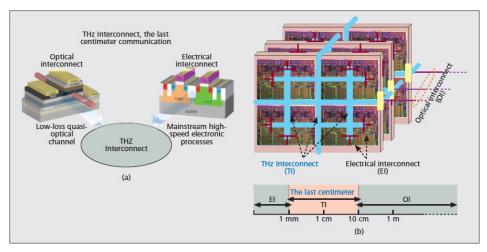
Utilize the diverse synaptic responses enabled by multi-terminal memtransistors for advanced learning paradigms informed by Threadwork co-design

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7

THz interconnects: Bridging the Optical and Electrical

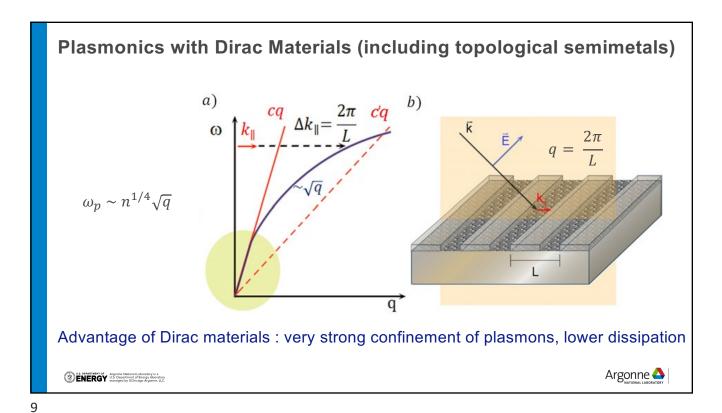


Dissipation becomes prohibitive using conventional interconnects for > 1mm in the THz regime.

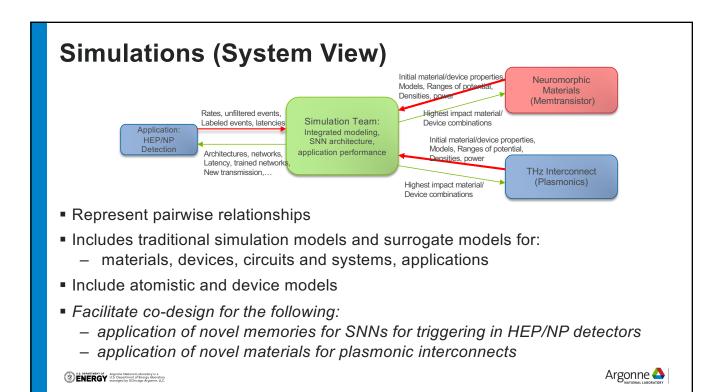
THz Plasmonic waveguides can bridge this gap

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Q.J. Gu, IEEE Communications Magazine p.206 April 2015. Argonne 📤



Example of a Plasmonic Interconnect Metallo-Dielectrically loaded dielectric laser plasmonic waveguides Plasmonic Driving electronics modulators Plasmonic Necessary electronics photodetectors Plasmonic chip-to-chip interconnect array CMOS chips with integrated driving electronics at the outputs feed their signals directly into a plasmonic modulator, which encodes the electrical signal onto a surface plasmon polariton. The signal is then transmitted over a dielectrically loaded plasmonic waveguide and received in a plasmonic photodetector. Adapted from A. Melikyan et al. ICTON'2012. J. Leuthold et al., Optics and Photonic News, May 2013. U.S. DEPARTMENT OF Argonne National Laboratory is a ENERGY U.S. Department of Energy laboratory managed by UChicago Argonne, LLC. Argonne 📤 10



Co-design Activities (Opportunities)

Optimized Spiking Neural Network Architectures for novel devices

- density, power
- continuous learning
- rich multi-terminal interconnections

Optimized Devices for Spiking Neural Network Architectures

- native spike processing in "Dual-gated Gaussian Hetero-junction Ts"
- dense layouts and crossbars
- large dynamic range
- synaptic responses
- plasticity

Multi-level optimization for Plasmonics

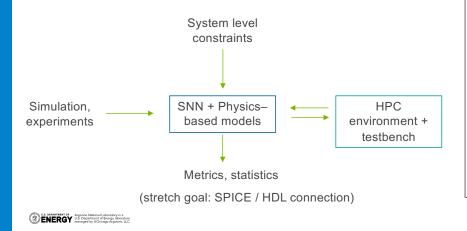
- materials systems combinations
- angles for design (performance, system implications)
- system capability optimization





Demonstrating and Benchmarking Non-trivial Computing

Extend SNNs to implement gating mechanisms that will allow context-dependent processing and learning as well as explore non-local / volume modulation leveraging the different length scales of plasmonic and memtransistor devices



Key ideas:

Current design tools cannot incorporate emergent technologies

Custom models can be run on leadership computing facilities in a massively parallel fashion

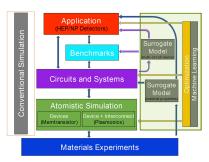
Models will be integrated to optimization engines to optimize over the design space (materials, devices, limited network architecture)



13

Accelerating Exploration with Surrogate Models

- Probabilistic machine learning-based surrogates that capture the heterogeneity and complexity of the data while accounting for the noise and uncertainty.
- Information-theoretic and Sparse Bayesian neural network with physics-informed constraints (wherever possible) will the leveraged for surrogate modeling.
- Active learning approaches (traditional Bayesian optimization, Monte Carlo tree-search) that can be used for mixed-integer optimization in the simulation campaign.
- Implemented and scaled on HPC through the Auto-ML framework DeepHyper.
- Interfaced at various stages (atomistic simulations, circuits, benchmarks and application).



Surrogate models

y
output:
weights:
(with distribution)
hidden layer:
weights:
(with distribution)
input:

Probabilistic and Physics-Informed

Multi-objective Optimization at Scale

Deeptyper

Deeptyper

Hyperparameter

Hyperparameter

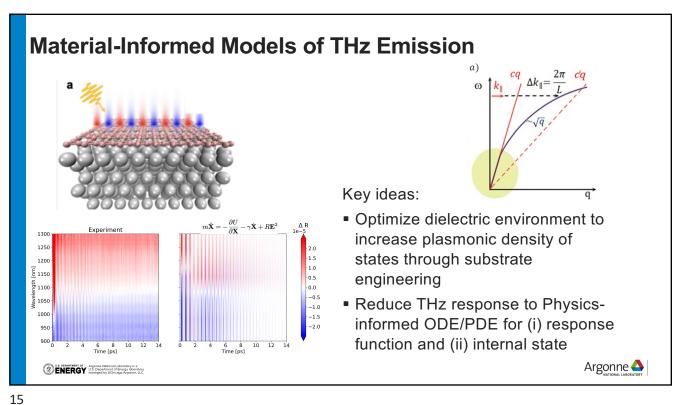
Hyperparameter

AMBS
AAC, random
DEAP, etc

RL with A2C,
A2C, random
MIGMALLMEALAGOT

MIGMALLMEALAGO

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