Memory & Network Design for Exascale Data Movement

Why data movement matters?
- Short answer: well, since you’re here…
- Formal answer: data movement is NOT as easily parallelizable as pure computation, it cannot be addressed by simply investing more resources. But instead, it’s important to know where to invest your resources, and how.

Key factors:
- Interconnect Network: through which data is moved
- Memory System: where data is stored, and manipulated

Memory System & Network
- What are the effects of different memory access patterns on different network parameters for a given problem size?
- What are the trade-offs when designing a system targeting one/multiple types of workloads?

Simulation Tool: SST [1]
- Simulation Set-up:
  From top level, the simulator is setup as a set of endpoints connected by interconnect network. Each endpoint consists of several Miranda cores and has a complete memory hierarchy and a Mesh router that talks to the network. The Miranda cores will generate memory access requests, which will then be transferred through the network.

Simulation Results:
- Some more details:

[1] SST stands for Structural Simulation Toolkit, developed by Sandia National Lab. It provides fine-grained simulation components that allows users to simulate a variety of architecture designs in for a large scale system.

Interconnect Technology
(Work in progress)
- There’s a need for new interconnect topologies to achieve both scalability and efficiency for exascale data movement. Interconnect is not only about the topologies, but also related techniques (routing, rank mapping, etc.).
- Characterization & analysis of proposed topology: What do we expect from the new topology?
- Novel Interconnect Topologies & Techniques:

Simulation Tool: Booksim
- Simulation Set-up (booksim):
  Simulator is warmed up before measuring. Topology is fed into Booksim by a native file, each 7x7 is given equal credit. Dijkstra’s algorithm is used to build the routing table. This is not guaranteed to find the “right” route, but would at least provide the lower performance bound of proposed topology

- Power & Performance at Small Scale:

A Petersen graph with a concentration factor of 5 vs. a Hoffman-Singleton Graph, a 7x7 Torus and a 7x7 flattened butterfly network are also simulated in order to provide a baseline for performance and power. The result is shown as follows:

- Scalability:

Conclusion and Future Work
As we can see from the simulation results of SST, different workloads behave quite differently on different topologies, and it also varies across different network configurations. The preliminary Booksim simulation results show that our proposed interconnect technique has lower latency and power compared to traditional techniques, and we would like to further optimize and fully use it on a large scale.

My name is Shang Li, a second-year PhD student from University of Maryland. Currently, I’m working on exascale system & architecture design, and I also have broad research interests over memory system, VLSI design, and operating systems.

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